Low Voltage Intel® Xeon™ Processor at 1.60 GHz, 2.0 GHz and 2.4 GHz

Datasheet

Product Features

- Available at 1.60 GHz, 2.0 GHz and 2.4 GHz
- Dual-/Uni- processing support
- Binary compatible with applications running on previous members of Intel's IA32 microprocessor line
- Intel® NetBurst™ micro-architecture
- Hyper-Threading Technology
  - — Hardware support for multithreaded applications
- 400 MHz System bus (1.6 Ghz and 2.0 Ghz)
  - — Bandwidth up to 3.2 GBytes/second
- 533 MHz System bus (2.4 Ghz)
  - — Bandwidth up to 4.3 GBytes/second
- Rapid Execution Engine: Arithmetic Logic Units (ALUs) run at twice the processor core frequency
- Hyper Pipelined Technology
- Advance Dynamic Execution
  - — Very deep out-of-order execution
  - — Enhanced branch prediction
- Level 1 Execution Trace Cache stores 12 K micro-ops and removes decoder latency from main execution loops
- Level 1 of 8 Kbytes data cache
- 512 KB Advanced Transfer L2 Cache (on-die, full speed Level 2 cache) with 8-way associativity and Error Correcting Code (ECC)
- Enables system support of up to 64 Gbytes of physical memory
- Streaming SIMD Extensions 2 (SSE2)
  - — 144 new instructions for double-precision floating point operations, media/video streaming, and secure transactions
- Enhanced floating point and multimedia unit for enhanced video, audio, encryption, and 3D performance
- Power Management capabilities
  - — System Management mode
  - — Multiple low-power states
- Advanced System Management Features
  - — Thermal Monitor
  - — Machine Check Architecture (MCA)

The Low Voltage Intel® Xeon™ processor at 1.6 Ghz and 2.0 Ghz with 400 Mhz system bus and 2.4 Ghz with 533 Mhz system bus are designed for high-performance dual and single processor applications. Based on the Intel® NetBurst™ micro-architecture and the new Hyper-Threading Technology, it is binary compatible with previous Intel Architecture (IA-32) processors. The Low Voltage Intel Xeon processor is scalable to two processors in a multiprocessor system providing exceptional performance for applications running on advanced operating systems such as Windows XP*, Windows* 2000, Linux*, and UNIX*. The Low Voltage Intel Xeon processor delivers compute power at unparalleled value and flexibility for embedded applications. The Intel® NetBurst™ micro-architecture and Hyper-Threading Technology deliver outstanding performance and headroom for embedded applications, resulting in faster response times, support for more users, and improved scalability.

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Revision History

Date	Revision	Description
September 2003	005	• Updated Figure 3, Low Voltage and Current Projections in a Dual-Processor Configuration.
September 2003	004	• Added Vcc and Icc voltage and current specificaitons for 2.4 GHz. • Added system bus to core frequency ratio specifications for 2.4 GHz. • Added processor thermal design power specifications for 2.4 GHz. • Added Overshoot/undershoot specification for 2.4 GHz. • Added Table 1 and Figure 7 • Updated Tables: 2, 3, 7, 8, 13, 14, 15, 17 and 37 and Figure 11
April 2003	003	• Added V_{CC} and I_{CC} voltage and current specifications for 2.0 GHz. • Added system bus to core frequency ratio specifications for 2.0 GHz. • Added processor thermal design power specifications for 2.0 GHz. • Changed the PROCHOT# signal type.
November 2002	002	• Redefined AE28 and AE29 pins. • Added VID_V_{CC} Voltage and current specifications.
September 2002	001	Initial release of this document.

1.0 Introduction

The Low Voltage Intel® Xeon™ processor is based on the Intel® NetBurst™ micro-architecture, which operates at significantly higher clock speeds and delivers performance levels that are significantly higher than previous generations of IA-32 processors. While based on the Intel NetBurst micro-architecture, it maintains the tradition of compatibility with IA-32 software.

The Intel NetBurst micro-architecture features begin with innovative techniques that enhance processor execution such as Hyper Pipelined Technology, a Rapid Execution Engine, Advanced Dynamic Execution, enhanced Floating Point and Multimedia unit, and Streaming SIMD Extensions 2 (SSE2). The Hyper Pipelined Technology doubles the pipeline depth in the processor, allowing the processor to reach much higher core frequencies. The Rapid Execution Engine allows the two integer ALUs in the processor to run at twice the core frequency, which allows many integer instructions to execute in one half of the internal core clock period. The Advanced Dynamic Execution improves speculative execution and branch prediction internal to the processor. The floating point and multi-media units have been improved by making the registers 128 bits wide and adding a separate register for data movement. Finally, SSE2 adds 144 new instructions for double-precision floating point, SIMD integer, and memory management for improvements in video/multimedia processing, secure transactions, and visual internet applications.

Also part of the Intel NetBurst micro-architecture, the system bus and caches on the Low Voltage Intel Xeon processor provide tremendous throughput for embedded applications. The 400/533 MHz system bus provides a high-bandwidth pipeline to the system memory and I/O. It is a quad-pumped bus running off a 100/133 MHz system bus clock making 3.2/4.3 Gigabytes per second (3,200/4,300 Megabytes per second) data transfer rates possible. The Execution Trace Cache is a level 1 cache that stores approximately twelve thousand decoded micro-operations, which removes the decoder latency from the main execution path and increases performance. The Advanced Transfer Cache is a 512 KB on-die level 2 cache running at the speed of the processor core providing increased bandwidth over previous micro-architectures.

In addition to the Intel NetBurst micro-architecture, the Low Voltage Intel Xeon processor includes a ground breaking new technology called Hyper-Threading technology, which enables multi-threaded software to execute tasks in parallel within the processor resulting in a more efficient, simultaneous use of processor resources. Embedded applications may realize increased performance from Hyper-Threading technology today through software and processor evolution. The combination of Intel NetBurst micro-architecture and Hyper-Threading technology delivers outstanding performance, throughput, and headroom for peak software workloads resulting in faster response times and improved scalability.

The Low Voltage Intel Xeon processor is intended for high performance embedded systems with up to two processors on a single bus. The processor supports both uni- and dual-processor designs and includes manageability features.

The Low Voltage Intel Xeon processor is packaged in a 604-pin Flip Chip Micro-Pin Grid Array (FC-µPGA2) package, and utilizes a surface mount ZIF socket with 604 pins. Mechanical components used for attaching thermal solutions to the baseboard should have a high degree of commonality with the thermal solution components enabled for the Low Voltage Intel Xeon processor. Heatsinks and retention mechanisms have been designed with manufacturability as a high priority. Hence, mechanical assembly may be completed from the top of the baseboard.

The Low Voltage Intel Xeon processor uses a scalable system bus protocol referred to as the “system bus” in this document. The processor system bus utilizes a split-transaction, deferred reply protocol similar to that introduced by the Intel® Pentium® Pro processor system bus, but is not

compatible with the Pentium Pro processor system bus. The system bus uses Source-Synchronous Transfer (SST) of address and data to improve performance, and transfers data four times per bus clock (4X data transfer rate). Along with the 4X data bus, the address bus may deliver addresses two times per bus clock and is referred to as a 'double-clocked' or 2X address bus. In addition, the Request Phase completes in one clock cycle. Working together, the 4X data bus and 2X address bus provide a data bus bandwidth of up to 3.2/4.3 Gigabytes per second. Finally, the system bus also introduces transactions that are used to deliver interrupts. For a list of features for each processor, see Table 1 below.

Signals on the system bus use Assisted GTL+ (AGTL+) level voltages which are fully described in the appropriate platform design guide (refer to Section 1.3).

Table 1. Features Comparison for Low Voltage Intel® Xeon™ Processors

Frequency	# of supported Systematic Agent	L2 Advanced Transfer Cache	Front Side Bus Frequency	Intel Hyper-Threading Technology	Package	Socket
1.60 GHz	1 - 2	512-KB	400 MHz	Yes	FC-µPGA2 (604 pins)	604-pin
2.0 GHz	1 - 2	512-KB	400 MHz	Yes	FC-µPGA2 (604 pins)	604-pin
2.4 GHz	1 - 2	512-KB	533 MHz	Yes	FC-µPGA2 (604 pins)	604-pin

1.1 Terminology

A '#' symbol after a signal name refers to an active low signal, indicating a signal is in the asserted state when driven to a low level. For example, when RESET# is low, a reset has been requested. Conversely, when NMI is high, a nonmaskable interrupt has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as *address* or *data*), the '#' symbol implies that the signal is inverted. For example, D[3:0] = 'HLHL' refers to a hex 'A', and D[3:0]# = 'LHLH' also refers to a hex 'A' (H= High logic level, L= Low logic level).

"System bus" refers to the interface between the processor, system core logic (the chipset components), and other bus agents. The system bus is a multiprocessing interface to processors, memory, and I/O. For this document, "system bus" is used as the generic term for the Intel® Xeon™ processor scalable system bus.

1.1.1 Processor Packaging Terminology

Commonly used terms are explained here for clarification:

- **604-pin socket** - The 604-pin socket contains an additional contact to accept the additional keying pin on the Low Voltage Intel Xeon processor in the FC-µPGA2 packages at pin location AE30. The 604-pin socket may also accept processors with the INT-mPGA package. Since the additional contact for pin AE30 is electrically inert, the 604-pin socket may not have a solder ball at this location. Therefore, the additional keying pin may not require a baseboard via nor a surface-mount pad. See the *604-Pin Socket Design Guidelines* for details regarding this socket.
- **Integrated Heat Spreader (IHS)** - The surface used to attach a heatsink or other thermal solution to the processor.

- **OEM** - Original Equipment Manufacturer.
- **Processor core** - The processor's execution engine. All AC timing and signal integrity specifications are to the pads of the processor core.
- **Retention mechanism** - The support components that are mounted through the baseboard to the chassis to provide mechanical retention for the processor and heatsink assembly.

1.2 State of Data

The data contained in this document is subject to change. It is the best information that Intel is able to provide at the publication date of this document.

1.3 References

The reader of this specification should also be familiar with material and concepts presented in the following documents:

Document	Intel Order Number[1]
AP-485, Intel® Processor Identification and the CPUID Instruction	241618
IA-32 Intel ® Architecture Software Developer's Manual • *Volume I: Basic Architecture* • *Volume II: Instruction Set Reference* • *Volume III: System Programming Guide*	 245470 245471 245472
Low Voltage Intel® Xeon™ Processor Thermal Design Guide	273764
604 -Pin Socket Design Guidelines	
Intel® Xeon™ Processor Specification Update	249678
Intel® Xeon™ Processor with 512 KB L2 Cache and Intel® E7500 Chipset Platform Design Guide	298649
Intel® Xeon™ Processor with 512 KB L2 cache and Intel ® E7500/E7501 Chipset Platform Design Guide-Addendum for Embedded Applications	273707
CK00 Clock Synthesizer/Driver Design Guidelines	249206
VRM 9.0 DC-DC Converter Design Guidelines	249205
VRM 9.1 DC-DC Converter Design Guidelines	298646
Dual Intel® Xeon™ Processor Voltage Regulator Down (VRD) Design Guidelines	298644
ITP700 Debug Port Design Guide	249679
Intel® Xeon™ Processor with 512 KB L2 Cache System Compatibility Guidelines	298645

NOTES:
1. Contact your Intel representative for the latest revision of documents without order numbers.
2. The signal integrity models are in IBIS format.

Document	Intel Order Number[1]
Low Voltage Intel® Xeon™ Processor Signal Integrity Models[2]	
Intel® Xeon™ Processor with 512 KB L2 Cache Mechanical Models in ProE Format*	http://developer.intel.com
Intel® Xeon™ Processor with 512 KB L2 Cache Mechanical Models in IGES Format*	http://developer.intel.com
Intel® Xeon™ Processor with 512 KB L2 Cache Core Boundary Scan Descriptor Language (BSDL) Model	http://developer.intel.com

NOTES:
1. Contact your Intel representative for the latest revision of documents without order numbers.
2. The signal integrity models are in IBIS format.

2.0 Electrical Specifications

2.1 System Bus and GTLREF

Most Low Voltage Intel® Xeon™ processor system bus signals use Assisted Gunning Transceiver Logic (AGTL+) signaling technology. This signaling technology provides improved noise margins and reduced ringing through low voltage swings and controlled edge rates. The processor termination voltage level is V_{CC}, the operating voltage of the processor core. The use of a termination voltage that is determined by the processor core allows better voltage scaling on the processor system bus. Because of the speed improvements to data and address busses, signal integrity and platform design methods become more critical than with previous processor families.

The AGTL+ inputs require a reference voltage (GTLREF) that is used by the receivers to determine if a signal is a logical 0 or a logical 1. GTLREF must be generated on the baseboard (See Table 12 for GTLREF specifications). Termination resistors are provided on the processor silicon and are terminated to its core voltage (V_{CC}). The on-die termination resistors are a selectable feature and may be enabled or disabled through the ODTEN pin. For end bus agents, on-die termination may be enabled to control reflections on the transmission line. For middle bus agents, on-die termination must be disabled. Intel chipsets may also provide on-die termination, thus eliminating the need to terminate the bus on the baseboard for most AGTL+ signals. Refer to Section 2.12 for details on ODTEN resistor termination requirements.

Some AGTL+ signals do not include on-die termination and must be terminated on the baseboard. See Table 5 for details regarding these signals.

The AGTL+ signals depend on incident wave switching. Therefore timing calculations for AGTL+ signals are based on flight time as opposed to capacitive deratings. Analog signal simulation of the system bus, including trace lengths, is highly recommended when designing a system.

2.2 Power and Ground Pins

For clean on-chip power distribution, the Low Voltage Intel Xeon processor has 190 V_{CC} (power) and 189 V_{SS} (ground) inputs. All V_{CC} pins must be connected to the system power plane, while all V_{SS} pins must be connected to the system ground plane. The processor V_{CC} pins must be supplied the voltage determined by the processor VID (Voltage ID) pins.

2.3 Decoupling Guidelines

Due to its large number of transistors and high internal clock speeds, the processor is capable of generating large average current swings between low and full power states. This may cause voltages on power planes to sag below their minimum values when bulk decoupling is not adequate. Larger bulk storage (C_{BULK}), such as electrolytic capacitors, supply current during longer lasting changes in current demand by the component, such as coming out of an idle condition. Similarly, they act as a storage well for current when entering an idle condition from a running condition. Care must be taken in the baseboard design to ensure that the voltage provided to the processor remains within the specifications listed in Table 7. Failure to do so may result in timing violations or reduced lifetime of the component. For further information and guidelines, refer to the appropriate platform design guidelines.

2.3.1 V_{CC} Decoupling

Regulator solutions need to provide bulk capacitance with a low Effective Series Resistance (ESR) and the baseboard designer must ensure a low interconnect resistance from the regulator (or VRM pins) to the 604-pin socket. Bulk decoupling may be provided on the voltage regulation module (VRM) to meet help meet the large current swing requirements. The remaining decoupling is provided on the baseboard. The power delivery path must be capable of delivering enough current while maintaining the required tolerances (defined in Table 7). For further information regarding power delivery, decoupling, and layout guidelines, refer to the appropriate platform design guidelines.

2.3.2 System Bus AGTL+ Decoupling

The Intel® Xeon™ processor integrates signal termination on the die as well as part of the required high frequency decoupling capacitance on the processor package. However, additional high frequency capacitance must be added to the baseboard to properly decouple the return currents from the system bus. Bulk decoupling must also be provided by the baseboard for proper AGTL+ bus operation. Decoupling guidelines are described in the appropriate platform design guidelines.

2.4 System Bus Clock (BCLK[1:0]) and Processor Clocking

BCLK[1:0] directly controls the system bus interface speed as well as the core frequency of the processor. As in previous generation processors, the processor core frequency is a multiple of the BCLK[1:0] frequency. The maximum processor bus ratio multiplier may be set during manufacturing. The default setting may equal the maximum speed for the processor.

The BCLK[1:0] inputs directly control the operating speed of the system bus interface. The processor core frequency is configured during reset by using values stored internally during manufacturing. The stored value sets the highest bus fraction at which the particular processor may operate.

Clock multiplying within the processor is provided by the internal PLL, which requires a constant frequency BCLK[1:0] input with exceptions for spread spectrum clocking. Processor DC and AC specifications for the BCLK[1:0] inputs are provided in Table 7 and Table 12, respectively. These specifications must be met while also meeting signal integrity requirements as outlined in Chapter 3.0. The processor utilizes a differential clock. Details regarding BCLK[1:0] driver specifications are provided in the *CK00 Clock Synthesizer/Driver Design Guidelines*. Table 1 contains the supported bus fraction ratios and their corresponding core frequencies.

Table 2. Front Side Bus-to-Core Frequency Ratio

Front Side Bus-to-Core Frequency Ratio	Front Side Bus Frequency	Core Frequency
1/16	100 MHz	1.60 GHz
1/18	133 MHz	2.40 GHz
1/20	100 MHz	2.0 GHz

2.4.1 Bus Clock

The system bus frequency is set to the maximum supported by the individual processor. BSEL[1:0] are outputs used to select the system bus frequency. Table 3 defines the possible combinations of the signals and the frequency associated with each combination. The frequency is determined by the processor(s), chipset, and clock synthesizer. All system bus agents must operate at the same frequency. Individual processors may only operate at their specified system bus clock frequency.

Baseboards designed for the Intel® Xeon™ processor employ a 100/133 MHz system bus clock. On these baseboards, BSEL[1:0] are considered 'reserved' at the processor socket.

Table 3. System Bus Clock Frequency Select Truth Table for BSEL[1:0]

BSEL1	BSEL0	Bus Clock Frequency
L	L	100 MHz
L	H	133 MHz
H	L	Reserved
H	H	Reserved

2.5 PLL Filter

V_{CCA} and $V_{CCIOPLL}$ are power sources required by the processor PLL clock generator. This requirement is identical to that of the Intel Xeon processor. Since these PLLs are analog in nature, they require quiet power supplies for minimum jitter. Jitter is detrimental to the system: it degrades external I/O timings as well as internal core timings (i.e., maximum frequency). To prevent this degradation, these supplies must be low pass filtered from V_{CC}. A typical filter topology is shown in Figure 1.

The AC low-pass requirements, with input at V_{CC} and output measured across the capacitor (C_A or C_{IO} in Figure 1), is as follows:

- < 0.2 dB gain in pass band
- < 0.5 dB attenuation in pass band < 1 Hz (see DC drop in next set of requirements)
- > 34 dB attenuation from 1 MHz to 66 MHz
- > 28 dB attenuation from 66 MHz to core frequency

The filter requirements are illustrated in Figure 2. For recommendations on implementing the filter refer to the appropriate platform design guidelines.

Figure 1. Typical $V_{CCIOPLL}$, V_{CCA} and V_{SSA} Power Distribution

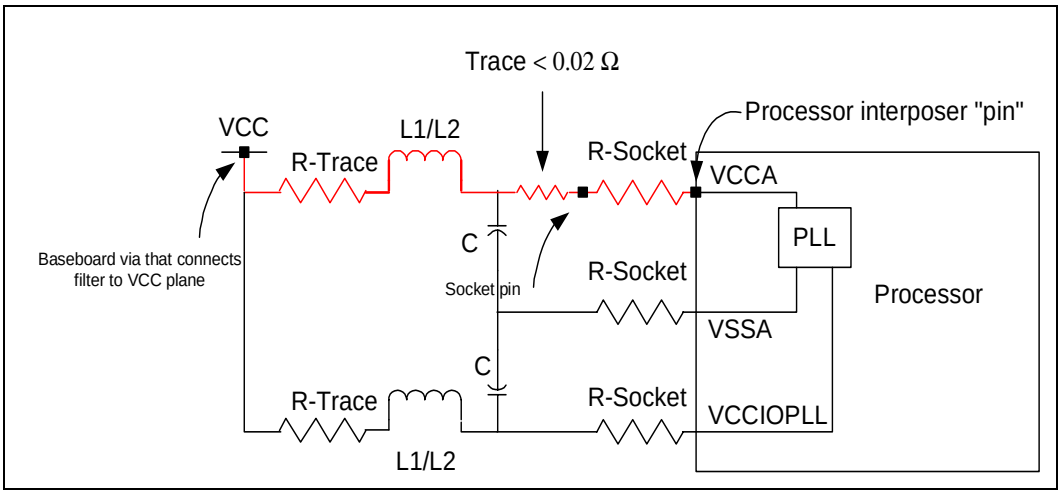
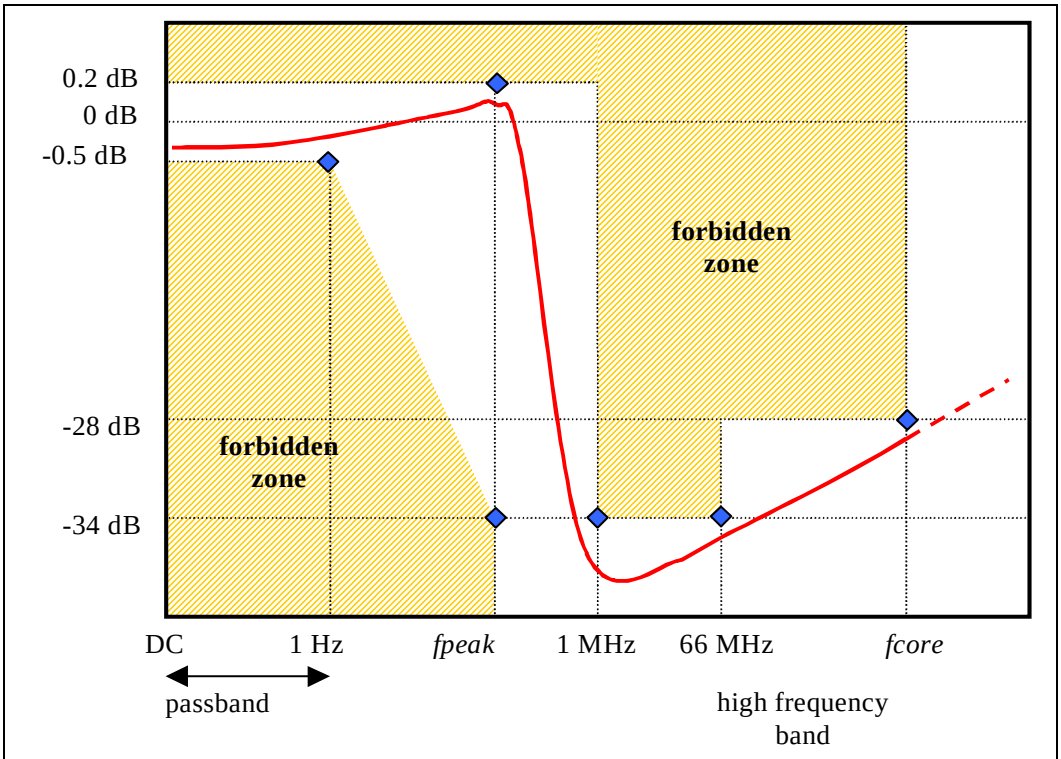


Figure 2. Phase Lock Loop (PLL) Filter Requirements



NOTES:
1. Diagram not to scale.
2. No specifications for frequencies beyond f_{core} (core frequency).
3. f_{peak}, if existent, should be less than 0.05 MHz.

2.5.1 Mixing Processors

Intel only supports those processor combinations operating with the same system bus frequency, core frequency, VID settings, and cache sizes. Not all operating systems may support multiple processors with mixed frequencies. Intel does not support or validate operation of processors with different cache sizes. Mixing processors of different steppings but the same model (as per CPUID instruction) is supported, and is outlined in the *Intel® Xeon™ Processor Specification Update*. Additional details are provided in AP-485, the *Intel Processor Identification and the CPUID Instruction* application note.

Unlike previous Intel Xeon processors, the Low Voltage Intel Xeon processor does not sample the pins IGNNE#, LINT[0]/INTR, LINT[1]/NMI, and A20M# to establish the core to system bus ratio. Rather, the processor runs at its tested frequency at initial power-on. When the processor needs to run at a lower core frequency, as must be done when a higher speed processor is added to a system that contains a lower frequency processor, the system BIOS is able to effect the change in the core to system bus ratio.

2.6 Voltage Identification

The VID specification for the processor is defined in this datasheet, and is supported by power delivery solutions designed according to the *Dual Intel® Xeon™ Processor Voltage Regulator Down (VRD) Design Guidelines, VRM 9.0 DC-DC Converter Design Guidelines*, and *VRM 9.1 DC-DC Converter Design Guidelines*. The minimum voltage is provided in Table 7, and varies with processor frequency. This allows processors running at a higher frequency to have a relaxed minimum voltage specification. The specifications have been set such that one voltage regulator design may work with all supported processor frequencies.

Note that the VID pins may drive valid and correct logic levels when the Intel® Xeon™ processor is provided with a valid voltage applied to the VID_V_{CC} pins. **VID_V_{CC} must be correct and stable prior to enabling the output of the VRM that supplies V_{CC}. Similarly, the output of the VRM must be disabled before VID_V_{CC} becomes invalid**. Refer to Figure 16 for details.

The processor uses five voltage identification pins, VID[4:0], to support automatic selection of processor voltages. Table 4 specifies the voltage level corresponding to the state of VID[4:0]. In this table, a 1 refers to a high voltage and a 0 refers to low voltage level. When the processor socket is empty (VID[4:0] = 11111), or the VRD or VRM cannot supply the voltage that is requested, it must disable its voltage output. For further details, see the *Dual Intel® Xeon™ Processor Voltage Regulator Down (VRD) Design Guidelines, or VRM 9.0 DC-DC Converter Design Guidelines* or the *VRM 9.1 DC-DC Converter Design Guidelines*.

Table 4. Voltage Identification Definition

Processor Pins					
VID4	VID3	VID2	VID1	VID0	V_{CC_VID} (V)
1	1	1	1	1	VRM output off
1	1	1	1	0	1.100
1	1	1	0	1	1.125
1	1	1	0	0	1.150
1	1	0	1	1	1.175
1	1	0	1	0	1.200
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	1	1.375
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450
0	1	1	1	1	1.475
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575
0	1	0	1	0	1.600
0	1	0	0	1	1.625
0	1	0	0	0	1.650
0	0	1	1	1	1.675
0	0	1	1	0	1.700
0	0	1	0	1	1.725
0	0	1	0	0	1.750
0	0	0	1	1	1.775
0	0	0	1	0	1.800
0	0	0	0	1	1.825
0	0	0	0	0	1.850

2.6.1 Mixing Processors of Different Voltages

Mixing processors operating with different VID settings (voltages) is not supported and may not be validated by Intel.

2.7 Reserved Or Unused Pins

All Reserved pins must remain unconnected on the system baseboard. Connection of these pins to V_{CC}, V_{SS}, or to any other signal (including one another) may result in component malfunction or incompatibility with future processors. See Chapter 5.0 for a pin listing of the processor and for the location of all Reserved pins.

For reliable operation, unused inputs or bidirectional signals should always be connected to an appropriate signal level. In a system-level design, on-die termination has been included on the processor to allow signal termination to be accomplished by the processor silicon. Most unused AGTL+ inputs should be left as no connects, as AGTL+ termination is provided on the processor silicon. However, see Table 5 for details on AGTL+ signals that do not include on-die termination. Unused active high inputs should be connected through a resistor to ground (V_{SS}). Unused outputs may be left unconnected, however this may interfere with some TAP functions, complicate debug probing, and prevent boundary scan testing. A resistor must be used when tying bidirectional signals to power or ground. When tying any signal to power or ground, a resistor may also allow for system testability. For unused AGTL+ input or I/O signals, use pull-up resistors of the same value for the on-die termination resistors (R_{TT}). See Table 12.

TAP, Asynchronous GTL+ inputs, and Asynchronous GTL+ outputs do not include on-die termination. Inputs and all used outputs must be terminated on the baseboard. Unused outputs may be terminated on the baseboard or left unconnected. Note that leaving unused outputs unterminated may interfere with some TAP functions, complicate debug probing, and prevent boundary scan testing. Signal termination for these signal types is discussed in the *ITP700 Debug Port Design Guide*.

All TESTHI[6:0] pins should be individually connected to V_{CC} through a pull-up resistor which matches the trace impedance within ±10 Ω. TESTHI[3:0] and TESTHI[6:5] may all be tied together and pulled up to V_{CC} with a single resistor when desired. However, utilization of the boundary scan test may not be functional when these pins are connected together. TESTHI4 must always be pulled up independently from the other TESTHI pins. For optimum noise margin, all pull-up resistor values used for TESTHI[6:0] pins should have a resistance value within 20 percent of the impedance of the baseboard transmission line traces. For example, when the trace impedance is 50 W, then a pull-up resistor value between 40 and 60 W should be used. The TESTHI[6:0] termination recommendations provided in the *Low Voltage Intel® Xeon™ Processor Datasheet* are also suitable for the Intel® Xeon™ processor. However, Intel recommends new designs or designs undergoing design updates follow the trace impedance matching termination guidelines outlined in this section.

2.8 System Bus Signal Groups

In order to simplify the following discussion, the system bus signals have been combined into groups by buffer type. AGTL+ input signals have differential input buffers, which use GTLREF as a reference level. In this document, the term “AGTL+ Input” refers to the AGTL+ input group as well as the AGTL+ I/O group when receiving. Similarly, “AGTL+ Output” refers to the AGTL+ output group as well as the AGTL+ I/O group when driving.

With the implementation of a source synchronous data bus comes the need to specify two sets of timing parameters. One set is for common clock signals whose timings are specified with respect to rising edge of BCLK0 (ADS#, HIT#, HITM#, etc.) and the second set is for the source synchronous signals which are relative to their respective strobe lines (data and address) as well as

rising edge of BCLK0. Asynchronous signals are still present (A20M#, IGNNE#, etc.) and may become active at any time during the clock cycle. Table 5 identifies which signals are common clock, source synchronous and asynchronous.

Table 5. System Bus Signal Groups

Signal Group	Type	Signals[1]
AGTL+ Common Clock Input	Synchronous to BCLK[1:0]	BPRI#, BR[3:1]#[3, 4], DEFER#, RESET#[4], RS[2:0]#, RSP#, TRDY#
AGTL+ Common Clock I/O	Synchronous to BCLK[1:0]	ADS#, AP[1:0]#, BINIT#[7], BNR#[7], BPM[5:0]#[2], BR0#[2], DBSY#, DP[3:0]#, DRDY#, HIT#[7], HITM#[7], LOCK#, MCERR#[7]
AGTL+ Source Synchronous I/O	Synchronous to assoc. strobe	<table><tr><th>Signals</th><th>Associated Strobe</th></tr><tr><td>REQ[4:0]#,A[16:3]#[6]</td><td>ADSTB0#</td></tr><tr><td>A[35:17]#[5]</td><td>ADSTB1#</td></tr><tr><td>D[15:0]#, DBI0#</td><td>DSTBP0#, DSTBN0#</td></tr><tr><td>D[31:16]#, DBI1#</td><td>DSTBP1#, DSTBN1#</td></tr><tr><td>D[47:32]#, DBI2#</td><td>DSTBP2#, DSTBN2#</td></tr><tr><td>D[63:48]#, DBI3#</td><td>DSTBP3#, DSTBN3#</td></tr></table>
AGTL+ Strobes	Synchronous to BCLK[1:0]	ADSTB[1:0]#, DSTBP[3:0]#, DSTBN[3:0]#
Asynchronous GTL+ Input[4]	Asynchronous	A20M#[5], IGNNE#[5], INIT#[6], LINT0/INTR[5], LINT1/NMI[5], SMI#[6], SLP#, STPCLK#
Asynchronous GTL+ Output[4]	Asynchronous	FERR#, IERR#, THERMTRIP#
Asynchronous GTL+ Input/ Output[9]	Asynchronous	PROCHOT#
System Bus Clock	Clock	BCLK1, BCLK0
TAP Input[2]	Synchronous to TCK	TCK, TDI, TMS, TRST#
TAP Output[2]	Synchronous to TCK	TDO
Power/Other	Power/Other	BSEL[1:0], COMP[1:0], GTLREF, ODTEN, Reserved, SKTOCC#, TESTHI[6:0],VID[4:0], V_{CC}, V_{CCA}, $V_{CCIOPLL}$, V_{SSA}, V_{SS}, $V_{CCSENSE}$, $V_{SSSENSE}$, PWRGOOD, THERMDA, THERMDC. VID_V_{CC}[8]

NOTES:
1. Refer to Section 5.2 for signal descriptions.
2. These AGTL+ signal groups are not terminated by the processor. Refer the *ITP700 Debug Port Design Guide* and corresponding Design Guide for termination requirements and further details.
3. The Low Voltage Intel® Xeon™ processor utilizes only BR0# and BR1#. BR2# and BR3# are not driven by the processor but must be terminated to V_{CC}. For additional details regarding the BR[3:0]# signals, see Section 5.2 and Section 7.1 and the appropriate Platform Design Guidelines.
4. These signal groups are not terminated by the processor. Refer to the appropriate platform design guidelines and the I*TP700 Debug Port Design Guide* for termination recommendations.
5. The volume on these pins during active-to-inactive edge of RESET# determines the multiplier that the Phase Lock Loop (PLL) will use for internal core clock
6. The value of these pins during the active-to-inactive edge of RESET# to determine processor configuration options. See Section 7.1 for details.
7. These signals may be driven simultaneously by multiple agents (wired-OR).
8. VID_V_{CC} is required for correct operation of the Low Voltage Intel® Xeon™ Processor. Refer to Figure 16 for details.
9. It is an output only on the 1.60 GHz Low Voltage Intel® Xeon™ processor with CPUID of 0F27h.

2.9 Asynchronous GTL+ Signals

The Low Voltage Intel® Xeon™ processor does not utilize CMOS voltage levels on any signals that connect to the processor silicon. As a result, legacy input signals such as A20M#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, SMI#, SLP#, and STPCLK# utilize GTL+ input buffers. Legacy output FERR#/PBE# and other non-AGTL+ signals IERR#, and THERMTRIP# utilize GTL+ output buffers. PROCHOT# uses GTL+ input/output buffer. All of these asynchronous GTL+ signals follow the same DC requirements as AGTL+ signals, however the outputs are not driven high (during the logical 0-to-1 transition) by the processor (the major difference between GTL+ and AGTL+). Asynchronous GTL+ signals do not have setup or hold time specifications in relation to BCLK[1:0]. However, all of the asynchronous GTL+ signals are required to be asserted for at least two BCLKs in order for the processor to recognize them. See Table 11 and Table 16 for the DC and AC specifications for the asynchronous GTL+ signal groups.

2.10 Maximum Ratings

Table 6 lists the processor's maximum environmental stress ratings. Functional operation at the absolute maximum and minimum is neither implied nor ensured. The processor should not receive a clock while subjected to these conditions. Functional operating parameters are listed in the AC and DC tables. Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the processor contains protective circuitry to resist damage from static electric discharge, one should always take precautions to avoid high static voltages or electric fields.

Table 6. Processor Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
$T_{STORAGE}$	Processor storage temperature	-40	85	°C	2
V_{CC}	Any processor supply voltage with respect to V_{SS}	-0.3	1.75	V	1
$V_{inAGTL+}$	AGTL+ buffer DC input voltage with respect to V_{SS}	-0.1	1.75	V	
V_{inGTL+}	Async GTL+ buffer DC input voltage with respect to Vss	-0.1	1.75	V	
I_{VID}	Max VID pin current		5	mA	

NOTES:
1. This rating applies to any pin of the processor.
2. Contact Intel for storage requirements in excess of one year.

2.11 Processor DC Specifications

The processor DC specifications in this section are defined at the processor core (pads) unless noted otherwise. See Section 5.1 for the processor pin listings and Section 5.2 for the signal definitions. The voltage and current specifications for all versions of the processor are detailed in Table 7. For platform planning refer to Figure 3. Notice that the graphs include Thermal Design Power (TDP) associated with the maximum current levels. The DC specifications for the AGTL+ signals are listed in Table 9.

The system bus clock signal group is detailed in Table 7. The DC specifications for these signal group is listed in Table 10.

Table 7 through Table 12 list the processor DC specifications and are valid only while meeting specifications for case temperature (T_{CASE} as specified in Chapter 6.0), clock frequency, and input voltages. Care should be taken to read all notes associated with each parameter.

Table 7. Voltage and Current Specifications

Symbol	Parameter	Core Freq	Min	Typ	Max	VID	Unit	Notes
V_{CC}	V_{CC} for Low Voltage Intel Xeon processor core in a dual-processor configuration.	1.60 GHz 2.0 GHz 2.4 GHz	1.187 1.179 1.170	Refer to Figure 3.	1.274 1.270 1.265	1.3	V	1, 2, 3, 9, 10
VID_V_{CC}	VID supply voltage	All freq	3.135	3.3	3.465		V	11
I_{CC}	I_{CC} for Low Voltage Intel Xeon processor core in a dual-processor configuration.	1.60 GHz 2.0 GHz 2.4 GHz			30.4 35.7 40.9		A	3, 4
I_{CC_VID}	I_{CC} for VID power supply	All freq		100.0	122.5		mA	11
I_{CC_PLL}	I_{CC} for PLL power pins	All freq			60		mA	7
I_{CC_GTLREF}	I_{CC} for GTLREF pins	All freq			15		µA	8
I_{SGnt}/I_{SLP}	I_{CC} Stop-Grant/Sleep	All freq			10.1		A	5
I_{TCC}	I_{CC} TCC active	All freq			10.1		A	6

NOTES:

1. These voltages are targets only. A variable voltage source should exist on systems in the event that a different voltage is required. See Section 2.6 and Table 4 for more information.
2. The voltage specification requirements are measured across vias on the platform for the V_{CC_SENSE} and V_{SS_SENSE} pins close to the socket with a 100 MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1 milliohm minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.
3. The processor should not be subjected to any static V_{CC} level that exceeds the V_{CC_MAX} associated with any particular current. Moreover, Vcc should never exceed V_{CC_VID}. Failure to adhere to this specification may shorten the processor lifetime.
4. Maximum current is defined at V_{CC_MAX}.
5. The current specified is also for AutoHALT State.
6. The maximum instantaneous current the processor may draw while the thermal control circuit is active as indicated by the assertion of PROCHOT#.
7. This specification applies to the PLL power pins VCCA and VCCIOPLL. See Section 2.5 for details. This parameter is based on design characterization and is not tested
8. This specification applies to each GTLREF pin.
9. The loadlines specify voltage limits at the die measured at V_{CC_SENSE} and V_{SS_SENSE} pins. Voltage regulation feedback for voltage regulator circuits must be taken from processor V_{CC} and V_{SS} pins.
10. Adherence to this loadline specification is required to ensure reliable processor operation.
11. VID_V_{CC} is required for correct operation of the Low Voltage Intel® Xeon™ Processor VID and BSEL logic. Refer to Figure 16 for details.

Figure 3. Low Voltage Intel® Xeon™ Processor Voltage and Current Projections in a Dual-Processor Configuration

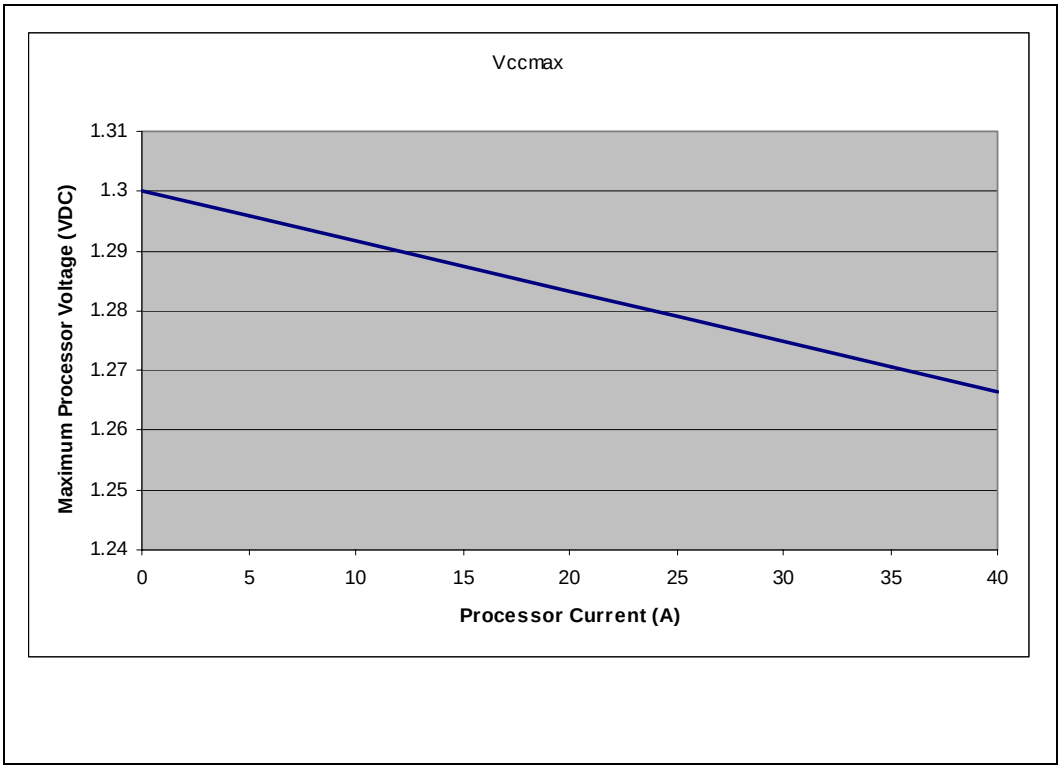


Table 8. System Bus Differential BCLK Specifications (Sheet 1 of 2)

Symbol	Parameter	Min	Typ	Max	Unit	Figure	Notes 1
V_L	Input Low Voltage	-.150	0.0	N/A	V	6	
V_H	Input High Voltage	0.660	0.710	0.850	V	6	
$V_{CROSS(abs)}$	Absolute Crossing Point	0.250	N/A	0.550	V	6, 8	2, 8
$V_{CROSS(rel)}$	Relative Crossing Point	0.250 + 0.5(V_{Havg} - 0.710)	N/A	0.550 + 0.5(V_{Havg} - 0.710)	V	6, 7	2, 3, 8 9
ΔV_{CROSS}	Range of Crossing Points	N/A	N/A	0.140	V	6, 8	2, 10
V_{OV}	Overshoot	N/A	N/A	VH + 0.3	V	6	4
V_{US}	Undershoot	-0.300	N/A	N/A	V	6	5

Table 8. System Bus Differential BCLK Specifications (Sheet 2 of 2)

V_{RBM}	Ringback Margin	0.200	N/A	N/A	V	6	6
V_{TM}	Threshold Margin	V_{CROSS} - 0.100	N/A	V_{CROSS} + 0.100	V	6	7

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Crossing voltage is defined as the instantaneous voltage value when the rising edge of BCLK0 equals the falling edge of BCLK1.
3. V_{Havg} is the statistical average of the V_H measured by the oscilloscope.
4. Overshoot is defined as the absolute value of the maximum voltage.
5. Undershoot is defined as the absolute value of the minimum voltage.
6. Ringback Margin is defined as the absolute voltage difference between the maximum Rising Edge Ringback and the maximum Falling Edge Ringback.
7. Threshold Region is defined as a region entered around the crossing point voltage in which the differential receiver switches. It includes input threshold hysteresis.
8. The crossing point must meet the absolute and relative crossing point specifications simultaneously.
9. V_{Havg} can be measured directly using “Vtop” on Agilent* scopes and “High” on Tektronix* scopes.
10. V_{CROSS} is defined as the total variation of all crossing voltages as defined in note 2.

Table 9. AGTL+ Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes[1, 7]
V_{IH}	Input High Voltage	1.10 * GTLREF	V_{CC}	V	2, 4, 6
V_{IL}	Input Low Voltage	0.0	0.90 * GTLREF	V	3, 6
V_{OH}	Output High Voltage	N/A	V_{CC}	V	4, 6
I_{OL}	Output Low Current	N/A	V_{CC} / ($0.50 * R_{TT\_min} + R_{ON\_min}$) = 50	mA	6
I_{HI}	Pin Leakage High	N/A	100	µA	9
I_{LO}	Pin Leakage Low	N/A	500	µA	8
R_{ON}	Buffer On Resistance	7	11	Ω	5, 7

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies and cache sizes.
2. V_{IH} is defined as the minimum voltage level at a receiving agent that may be interpreted as a logical high value.
3. V_{IL} is defined as the maximum voltage level at a receiving agent that may be interpreted as a logical low value.
4. V_{IH} and V_{ON} may experience excursions above V_{CC}. However, input signal drivers must comply with the signal quality specifications in Chapter 3.0.
5. Refer to the *Low Voltage Intel® Xeon™ Processor Signal Integrity Models* for I/V characteristics.
6. The V_{CC} referred to in these specifications refers to instantaneous V_{CC}.
7. V_{OL_MAX} of 0.450 V is ensured when driving into a test load as indicated in Figure 4, with R_{TT} enabled.
8. Leakage to V_{CC} with pin held at 300 mV.
9. Leakage to V_{SS} with pin held at V_{CC}.

Table 10. TAP and PWRGOOD Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes[1]
V_{HYS}	TAP Input Hysteresis	200	300		7
V_{T+}	TAP input low to high threshold voltage	0.5 * (V_{CC} + V_{HYS_MIN})	0.5 * (V_{CC} + V_{HYS_MAX})		4
V_{T-}	TAP input high to low threshold voltage	0.5 * (V_{CC} - V_{HYS_MAX})	0.5 * (V_{CC} - V_{HYS_MIN})		4
V_{OH}	Output High Voltage	N/A	V_{CC}	V	2, 4
I_{OL}	Output Low Current		40	mA	5, 6
I_{HI}	Pin Leakage High	N/A	100	µA	9
I_{LO}	Pin Leakage Low	N/A	500	µA	8
R_{ON}	Buffer On Resistance	8.75	13.75	Ω	3

NOTES:.
1. All outputs are open drain.
2. TAP signal group must meet the system signal quality specification in Chapter 3.0.
3. Refer to the *Low Voltage Intel® Xeon™ Processor Signal Integrity Models* for I/V characteristics.
4. The V_{CC} referred to in these specifications refers to instantaneous V_{CC}.
5. The maximum output current is based on maximum current handling capability of the buffer and is not specified into the test load.
6. V_{OL_MAX} of 0.300V is ensured when driving a test load.
7. V_{HYS} represents the amount of hysteresis, nominally centered about 0.5*V_{CC}, for all TAP inputs.
8. Leakage to V_{CC} with Pin held at 300 mV.
9. Leakage to V_{SS} with pin held at V_{CC}.

Table 11. Asynchronous GTL+ Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes[7]
V_{IH}	Input High Voltage	1.10 * GTLREF	V_{CC}	V	2, 4, 6
V_{IL}	Input Low Voltage	0.0	0.90 * GTLREF	V	3, 5
V_{OH}	Output High Voltage	N/A	Vcc	V	1, 4, 6
I_{OL}	Output Low Current		50	mA	7, 8
I_{HI}	Pin Leakage High	N/A	100	µA	10
I_{LO}	Pin Leakage Low	N/A	500	µA	9
R_{ON}	Buffer On Resistance	7	11	Ω	5

NOTES:
1. All outputs are open drain.
2. V_{IH} is defined as the minimum voltage level at a receiving agent that may be interpreted as a logical high value.
3. V_{IL} is defined as the maximum voltage level at a receiving agent that may be interpreted as a logical low value.
4. V_{IH} and V_{OH} may experience excursions above V_{CC}. However, input signal drivers must comply with the signal quality specifications in Chapter 3.0.
5. Refer to the *Low Voltage Intel® Xeon™ Processor Signal Integrity Models* for I/V characteristics.
6. The V_{CC} referred to in these specifications refers to instantaneous V_{CC}.
7. The maximum output current is based on maximum current handling capability of the buffer and is not specified into the test load.
8. V_{OL_MAX} of 0.450 V is ensured when driving into a test load as indicated in Figure 4, with R_{TT} enabled.
9. Leakage to V_{CC} with Pin held at 300 mV.
10. Leakage to V_{SS} with pin held at V_{CC}.

2.12 AGTL+ System Bus Specifications

Routing topologies are dependent on the number of processors supported and the chipset used in the design. Please refer to the appropriate platform design guidelines. In most cases, termination resistors are not required as these are integrated into the processor. See Table 5 for details on which AGTL+ signals do not include on-die termination.The termination resistors are enabled or disabled through the ODTEN pin. To enable termination, this pin should be pulled up to V_{CC} through a resistor and to disable termination, this pin should be pulled down to V_{SS} through a resistor. For optimum noise margin, all pull-up and pull-down resistor values used for the ODTEN pin should have a resistance value within 20 percent of the impedance of the baseboard transmission line traces. For example, when the trace impedance is 50 W, then a value between 40 and 60 W should be used. The processor's on-die termination must be enabled for the end agent only. Please refer to Table 12 for termination resistor values. For more details on platform design see the appropriate platform design guidelines.

Valid high and low levels are determined by the input buffers via comparing with a reference voltage called GTLREF.

Table 12 lists the GTLREF specifications. The AGTL+ reference voltage (GTLREF) should be generated on the baseboard using high precision voltage divider circuits. It is important that the baseboard impedance is held to the specified tolerance, and that the intrinsic trace capacitance for the AGTL+ signal group traces is known and well-controlled. For more details on platform design see the appropriate platform design guidelines.

Table 12. AGTL+ Bus Voltage Definitions

Symbol	Parameter	Min	Typ	Max	Units	Notes
GTLREF	Bus Reference Voltage	0.63 * V_{CC} - 2%	0.63 * V_{CC}	0.63 * V_{CC} + 2%	V	1, 2, 5
R_{TT}	Termination Resistance	45	50	55	Ω	3, 7
COMP[1:0]	COMP Resistance	49.55	50	50.45	Ω	4, 6, 7

NOTES:
1. The tolerances for this specification have been stated generically to enable system designer to calculate the minimum values across the range of V_{CC}.
2. GTLREF is generated from V_{CC} on the baseboard by a voltage divider of 1 percent resistors. Refer to the appropriate platform design guidelines for implementation details.
3. R_{TT} is the on-die termination resistance measured from V_{CC} to 1/3 V_{CC} at the AGTL+ output driver. Refer to the *Low Voltage Intel® Xeon™ Processor Cache Signal Integrity Models* for I/V characteristics.
4. COMP resistors are pull downs to V_{SS} provided on the baseboard with 1% tolerance. See the appropriate platform design guidelines for implementation details.
5. The V_{CC} referred to in these specifications refers to instantaneous V_{CC}.
6. The COMP resistance value varies by platform. Refer to the appropriate platform design guideline for the recommended COMP resistance value.
7. The values for R_{TT} and COMP noted as 'New Designs' apply to designs that are optimized for the Intel® Xeon™ processor. Refer to the appropriate platform design guideline for the recommended COMP resistance value.

2.13 System Bus AC Specifications

The processor system bus timings specified in this section are defined at the processor core (pads). See Section 5.0 for the pin listing and signal definitions.

Table 12 through Table 18 list the AC specifications associated with the processor system bus.

All AGTL+ timings are referenced to GTLREF for both 0 and 1 logic levels unless otherwise specified.

The timings specified in this section should be used in conjunction with the signal integrity models provided by Intel. These signal integrity models, which include package information, are available for the Intel® Xeon™ processor in IBIS format. AGTL+ layout guidelines are also available in the appropriate platform design guidelines.

Note: Care should be taken to read all notes associated with a particular timing parameter.

Table 13. System Bus Differential Clock Specifications

T# Parameter	Min	Nom	Max	Unit	Figure	Notes
Front Side Bus Clock Frequency (**400 MHz**)			100.0	MHz		1
Front Side Bus Clock Frequency (**533 MHz**)	130.07		133.33	MHz		1
T1: BCLK[1:0] Period (**400 MHz**)	10.00		10.20	ns	6	2
T1: BCLK[1:0] Period (**533 MHz**)	7.5		7.65	ns	6	2
T2: BCLK[1:0] Period Stability	N/A		150	ps		3, 4
T3: TPH BCLK[1:0] Pulse High Time (**400 MHz**)	3.94	5	6.12	ns	6	
T3: TPH BCLK[1:0] Pulse High Time (**533 MHz**)	2.955	3.75	4.59	ns	6	
T4: TPL BCLK[1:0] Pulse Low Time (**400 MHz**)	3.94	5	6.12	ns	6	
T4: TPL BCLK[1:0] Pulse Low Time (**533 MHz**)	2.955	3.75	4.59	ns	6	
T5: BCLK[1:0] Rise Time	175		700	ps	6	5
T6: BCLK[1:0] Fall Time	175		700	ps	6	5

NOTES:
1. The processor core clock frequency is derived from BCLK.
2. The period specified here is the average period. A given period may vary from this specification as governed by the period stability specification (T2).
3. For the clock jitter specification, refer to the *CK00 Clock Synthesizer/Driver Design Guidelines*.
4. In this context, period stability is defined as the worst case timing difference between successive crossover voltages. In other words, the largest absolute difference between adjacent clock periods must be less than the period stability.
5. Slew rate is measured between the 35% and 65% points of the clock swing (V_L and V_H)..

Table 14. System Bus Common Clock AC Specifications

T# Parameter	Min	Max	Unit	Figure	Notes[1, 2]
T10: Common Clock Output Valid Delay	0.12	1.27	ns	8	3
T11: Common Clock Input Setup Time	0.65	N/A	ns	8	4
T12: Common Clock Input Hold Time	0.40	N/A	ns	8	4
T13: RESET# Pulse Width	1.00	10.00	ms	11	5, 6, 7

NOTES:
1. Not 100% tested. Specified by design characterization.
2. All common clock AC timings for AGTL+ signals are referenced to the Crossing Voltage (V_{CROSS}) of the BCLK[1:0] at rising edge of BCLK0. All common clock AGTL+ signal timings are referenced at GTLREF at the processor core.
3. Valid delay timings for these signals are specified into the test circuit described in Figure 4 and with GTLREF at 0.63 * V_{CC} ± 2%.
4. Specification is for a minimum swing defined between AGTL+ V_{IL_MAX} to V_{IH_MIN}. This assumes an edge rate of 0.3 V/ns to 4.0 V/ns.
5. RESET# may be asserted (active) asynchronously, but must be deasserted synchronously.
6. This should be measured after V_{CC} and BCLK[1:0] become stable.
7. Maximum specification applies only while PWRGOOD is asserted.

Table 15. System Bus Source Synchronous AC Specifications (Sheet 1 of 2)

T# Parameter	Min	Max	Unit	Figure	Notes
T20: Source Sync. Output Valid Delay (first data/ address only)	0.20	1.3	ns	9, 10	1, 2, 3, 4
T21: TVBD Source Sync. Data Output Valid Before Data Strobe (**400 MHz)**	0.85		ns	10	1, 2, 3, 4, 7
T21: TVBD Source Sync. Data Output Valid Before Data Strobe (**533 MHz)**	0.535		ns	10	1, 2, 3, 4, 7
T22: TVAD Source Sync. Data Output Valid After Data Strobe (**400 MHz)**	0.85		ns	10	1, 2, 3, 4, 7
T22: TVAD Source Sync. Data Output Valid After Data Strobe (**533 MHz)**	0.535		ns	10	1, 2, 3, 4, 7
T23: TVBA Source Sync. Address Output Valid Before Address Strobe (**400 MHz)**	1.88		ns	9	1, 2, 3, 4, 7
T23: TVBA Source Sync. Address Output Valid Before Address Strobe (**533 MHz)**	1.360		ns	9	1, 2, 3, 4, 7
T24: TVAA Source Sync. Address Output Valid After Address Strobe (**400 MHz)**	1.88		ns	9	1, 2, 3, 4, 8
T24: TVAA Source Sync. Address Output Valid After Address Strobe (**533 MHz)**	1.360		ns	9	1, 2, 3, 4, 8
T25: TSUSS Source Sync. Input Setup Time	0.21		ns	9, 10	1, 2, 3, 5
T26: THSS Source Sync. Input Hold Time	0.21		ns	9, 10	1, 2, 3, 5
T27: TSUCC Source Sync. Input Setup Time to BCLK	0.65		ns	9, 10	1, 2, 3, 4, 6
T28: TFASS First Address Strobe to Second Address Strobe		1/2	BCLKs	9	1, 2, 3, 4, 9, 13
T29: TFDSS: First Data Strobe to Subsequent Strobes		n/4	BCLKs	10	1, 2, 3, 4, 10, 11, 13

Table 15. System Bus Source Synchronous AC Specifications (Sheet 2 of 2)

T# Parameter	Min	Max	Unit	Figure	Notes
T30: Data Strobe 'n' (DSTBN#) Output Valid Delay (**400 MHz)**	8.80	10.20	ns	10	1, 2, 3, 4, 12
T30: Data Strobe 'n' (DSTBN#) Output Valid Delay (**533 MHz)**	6.47	8.00	ns	10	1, 2, 3, 4, 12
T31: Address Strobe Output Valid Delay (**400 MHz)**	2.27	4.23	ns	9	1, 2, 3
T31: Address Strobe Output Valid Delay (**533 MHz)**	1.655	3.50	ns	9	1, 2, 3

NOTES:
1. Not 100% tested. Specified by design characterization.
2. All source synchronous AC timings are referenced to their associated strobe at GTLREF. Source synchronous data signals are referenced to the falling edge of their associated data strobe. Source synchronous address signals are referenced to the rising and falling edge of their associated address strobe. All source synchronous AGTL+ signal timings are referenced at GTLREF at the processor core.
3. Unless otherwise noted, these specifications apply to both data and address timings.
4. Valid delay timings for these signals are specified into the test circuit described in Figure 4 and with GTLREF at 0.63 * V_{CC} ± 2%.
5. Specification is for a minimum swing defined between AGTL+ V_{IL_MAX} to V_{IH_MIN}. This assumes an edge rate of 0.3 V/ns to 4.0 V/ns.
6. All source synchronous signals must meet the specified setup time to BCLK as well as the setup time to each respective strobe.
7. This specification represents the minimum time the data or address may be valid before its strobe. Refer to the appropriate platform design guidelines for more information on the definitions and use of these specifications.
8. This specification represents the minimum time the data or address may be valid after its strobe. Refer to the appropriate platform design guidelines for more information on the definitions and use of these specifications.
9. The rising edge of ADSTB# must come approximately 1/2 BCLK period (5 ns) after the falling edge of ADSTB#.
10. For this timing parameter, n = 1, 2, and 3 for the second, third, and last data strobes respectively.
11. The second data strobe (the falling edge of DSTBn#) must come approximately 1/4 BCLK period (2.5 ns) after the first falling edge of DSTBp#. The third data strobe (the falling edge of DSTBp#) must come approximately 2/4 BCLK period (5 ns) after the first falling edge of DSTBp#. The last data strobe (the falling edge of DSTBn#) must come approximately 3/4 BCLK period (7.5 ns) after the first falling edge of DSTBp#.
12. This specification applies only to DSTBN[3:0]# and is measured to the second falling edge of the strobe.
13. This specification reflects a typical value, not a minimum or maximum.

Table 16. Miscellaneous Signals+ AC Specifications

T# Parameter	Min	Max	Unit	Figure	Notes
T35: Async GTL+ input pulse width	2	N/A	BCLKs		1, 2, 3
T36: PWRGOOD to RESET# de-assertion time	1	10	ms	12	1, 2, 3
T37: PWRGOOD inactive pulse width	10	N/A	BCLKs	12	1, 2, 3, 4
T38: PROCHOT# pulse width	500		µs	14	1, 2, 3, 4, 5
T39: THERMTRIP# to Vcc Removal		0.5	s	15	

NOTES:
1. All AC timings for the Asynchronous GTL+ signals are referenced to the BCLK0 rising edge at Crossing Voltage (V_{CROSS}). All Asynchronous GTL+ signal timings are referenced at GTLREF.
2. These signals may be driven asynchronously.
3. Refer to Section 7.2 for additional timing requirements for entering and leaving low power states.
4. Refer to the PWRGOOD signal definition in Section 5.2 for more detail information on behavior of the signal.
5. Length of assertion for PROCHOT# does not equal TCC activation time. Time is required after the assertion and before the deassertion of PROCHOT# for the processor to enable or disable the TCC. This specification applies to PROCHOT# when asserted by the processor. A minimum pulse width of 500 µs is recommended when PROCHOT# is asserted by the system.

Table 17. System Bus AC Specifications (Reset Conditions)

T# Parameter	Min	Max	Unit	Figure	Notes
T45: Reset Configuration Signals (A[31:3]#, BR0#, INIT#, SMI#) Setup Time	4		BCLKs	11	1
T46: Reset Configuration Signals (A[31:3]#, INIT#, SMI#) Hold Time	2	20	BCLKs	11	2
T47: Reset Configuration Signal BR0# Hold Time	2	2	BCLKs	11	2

NOTES:
1. Before the de-assertion of RESET#
2. After the clock that de-asserts RESET#

Table 18. TAP Signal Group AC Specifications

T# Parameter	Min	Max	Unit	Figure	Notes1, 2, 8
T55: TCK Period	60.0		ns	5	
T56: TCK Rise Time		9.5	ns	5	3
T57: TCK Fall Time		9.5	ns	5	3
T58: TMS, TDI Rise Time		8.5	ns	5	3
T59: TMS, TDI Fall Time		8.5	ns	5	3
T61: TDI, TMS Setup Time	0		ns	13	4, 6
T62: TDI, TMS Hold Time	3.0		ns	13	4, 6
T63: TDO Clock to Output Delay	0.5	3.5	ns	13	5
T64: TRST# Assert Time	2.0		T_{TCK}	14	7

NOTES:
1. Not 100% tested. Specified by design characterization.
2. All AC timings for the TAP signals are referenced to the TCK signal at 0.5 * V_{CC} at the processor pins. All TAP signal timings (TMS, TDI, etc) are referenced at the 0.5 * V_{CC} processor pins.
3. Rise and fall times are measured from the 20% to 80% points of the signal swing.
4. Referenced to the rising edge of TCK.
5. Referenced to the falling edge of TCK.
6. Specification for a minimum swing defined between TAP 20% to 80%. This assumes a minimum edge rate of 0.5 V/ns.
7. TRST# must be held asserted for two TCK periods to ensure recognition by the processor.
8. It is recommended that TMS be asserted while TRST# is being deasserted

2.14 Processor AC Timing Waveforms

The following figures are used in conjunction with the AC timing tables, Table 12 through Table 18.

Note: For Figure 5 through Figure 14, the following apply:

1. All common clock AC timings for AGTL+ signals are referenced to the Crossing Voltage (V_{CROSS}) of the BCLK[1:0] at rising edge of BCLK0. All common clock AGTL+ signal timings are referenced at GTLREF at the processor core (pads).
2. All source synchronous AC timings for AGTL+ signals are referenced to their associated strobe (address or data) at GTLREF. Source synchronous data signals are referenced to the

falling edge of their associated data strobe. Source synchronous address signals are referenced to the rising and falling edge of their associated address strobe. All source synchronous AGTL+ signal timings are referenced at GTLREF at the processor core (pads).

3. All AC timings for AGTL+ strobe signals are referenced to BCLK[1:0] at V_{CROSS}. All AGTL+ strobe signal timings are referenced at GTLREF at the processor core (pads).
4. All AC Timing for he TAP signals are referenced to the TCK signal at 0.5 * V_{CC} at the processor pins. All TAP signal timings (TMS, TDI, etc.) are referenced at the 0.5 * V_{CC} at the processor core (pads).

Figure 4. Electrical Test Circuit

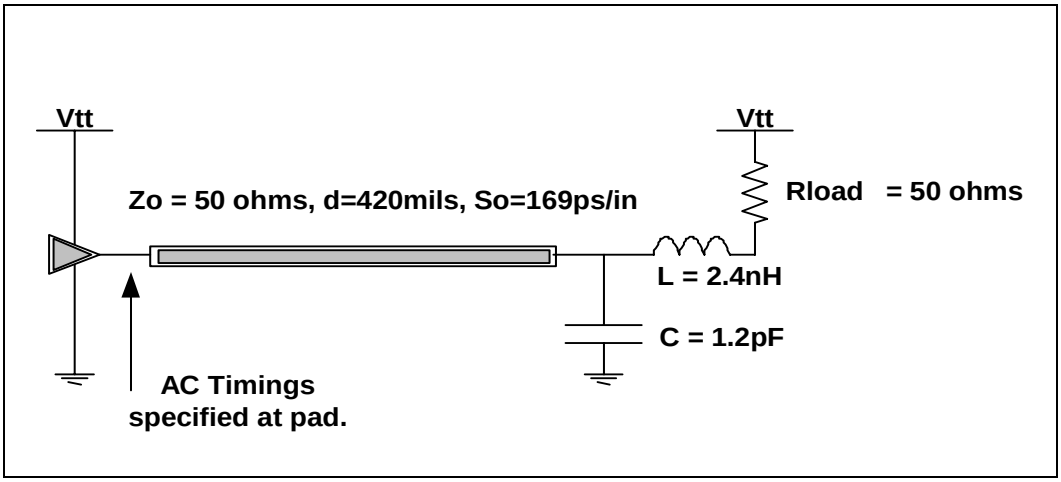


Figure 5. TCK Clock Waveform

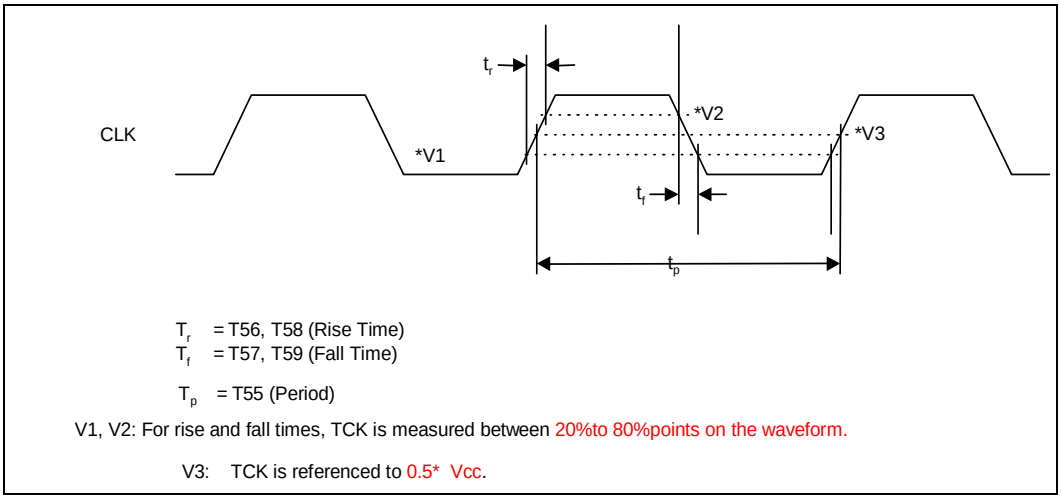
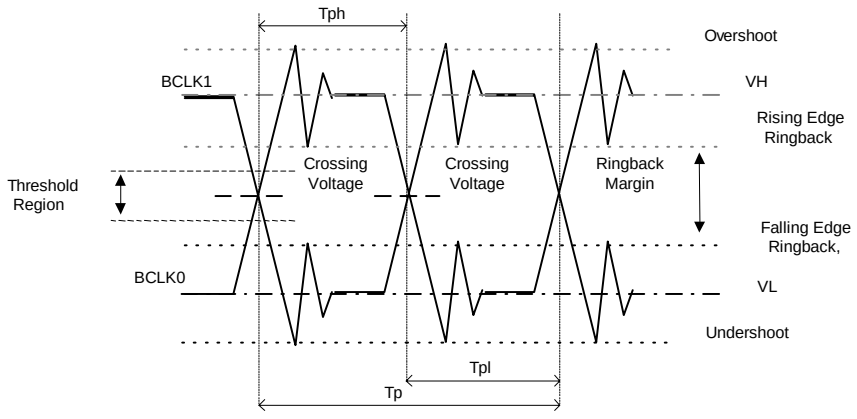


Figure 6. Differential Clock Waveform



Tp = T1 (BCLK[1:0] period)
T2 = BCLK[1:0] Period stability (not shown)
Tph =T3 (BCLK[1:0] pulse high time)
Tpl = T4 (BCLK[1:0] pulse low time)
T5 = BCLK[1:0] rise time through the threshold region
T6 = BCLK[1:0] fall time through the threshold region

Figure 7. Differential Clock Crosspoint Specification

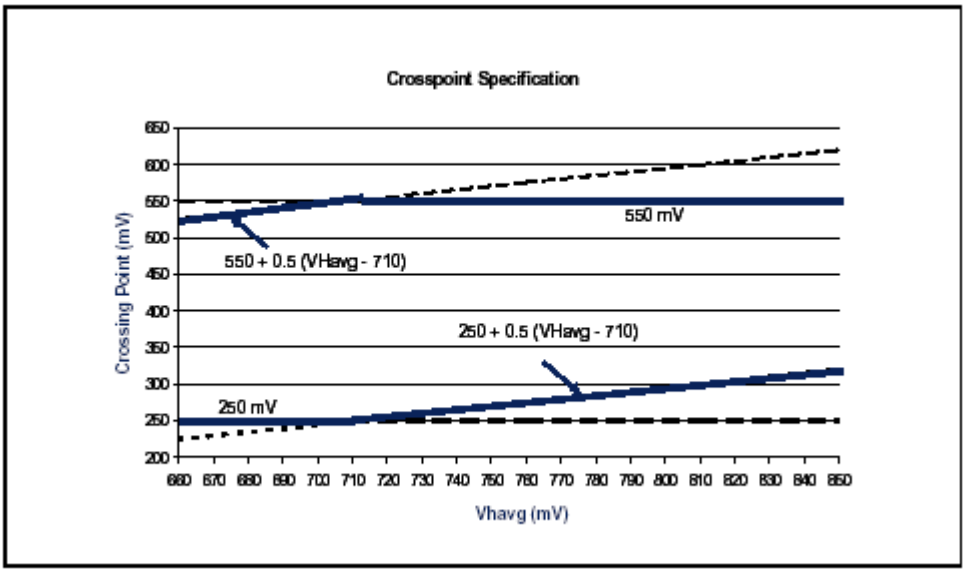


Figure 8. System Bus Common Clock Valid Delay Timing Waveform

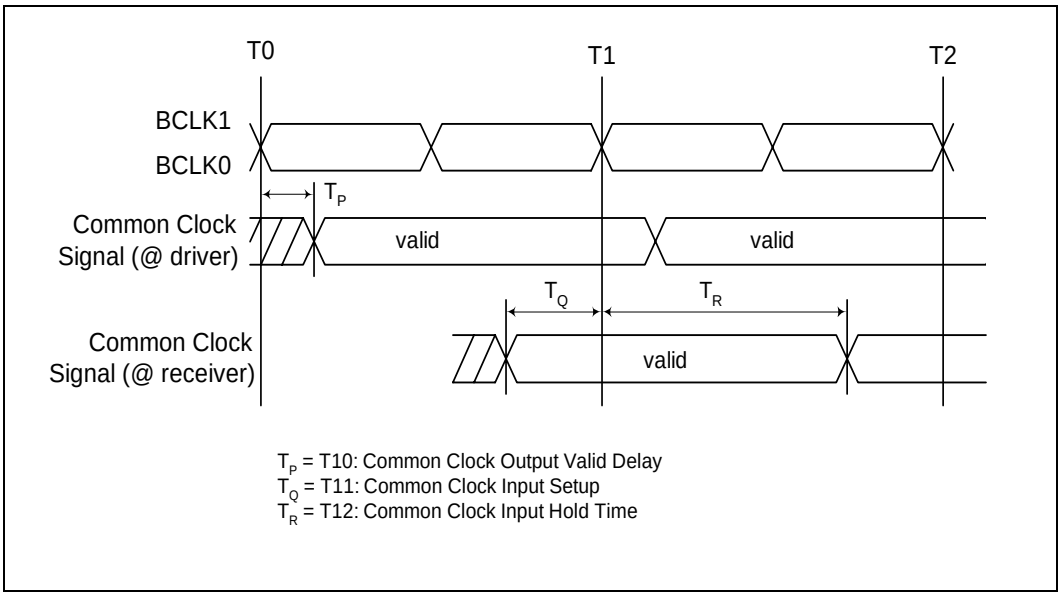


Figure 9. System Bus Source Synchronous 2X (Address) Timing Waveform

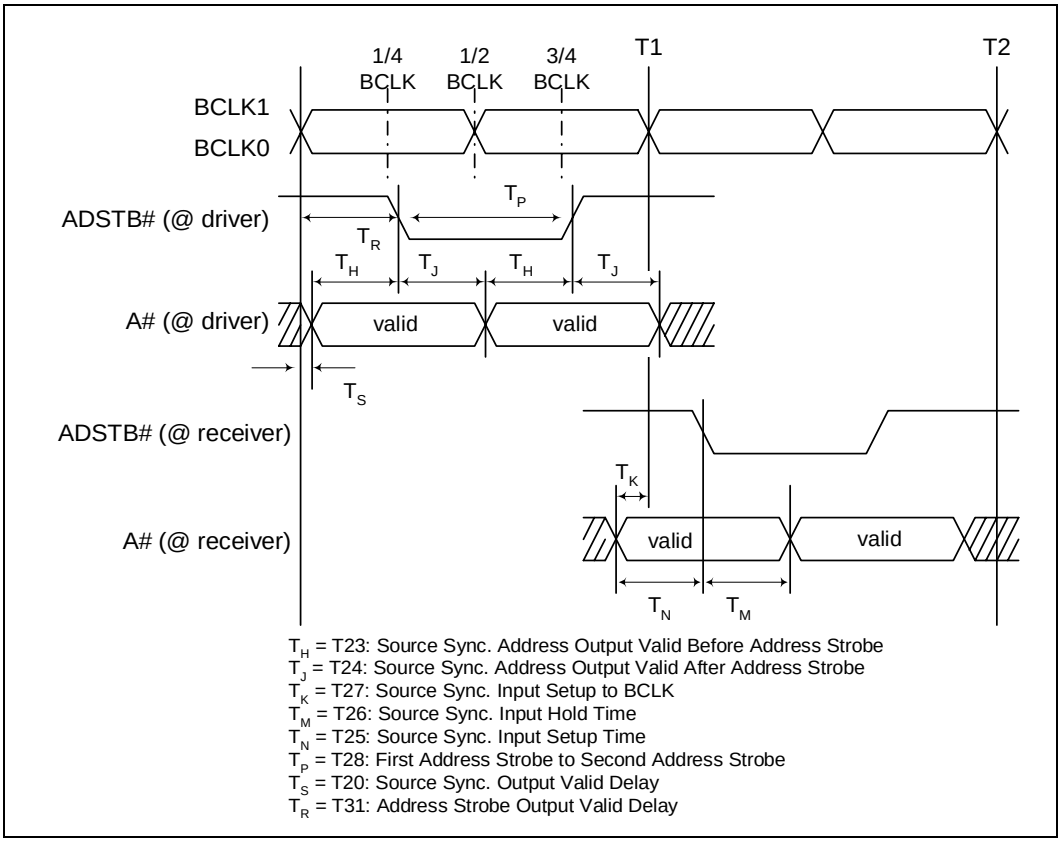
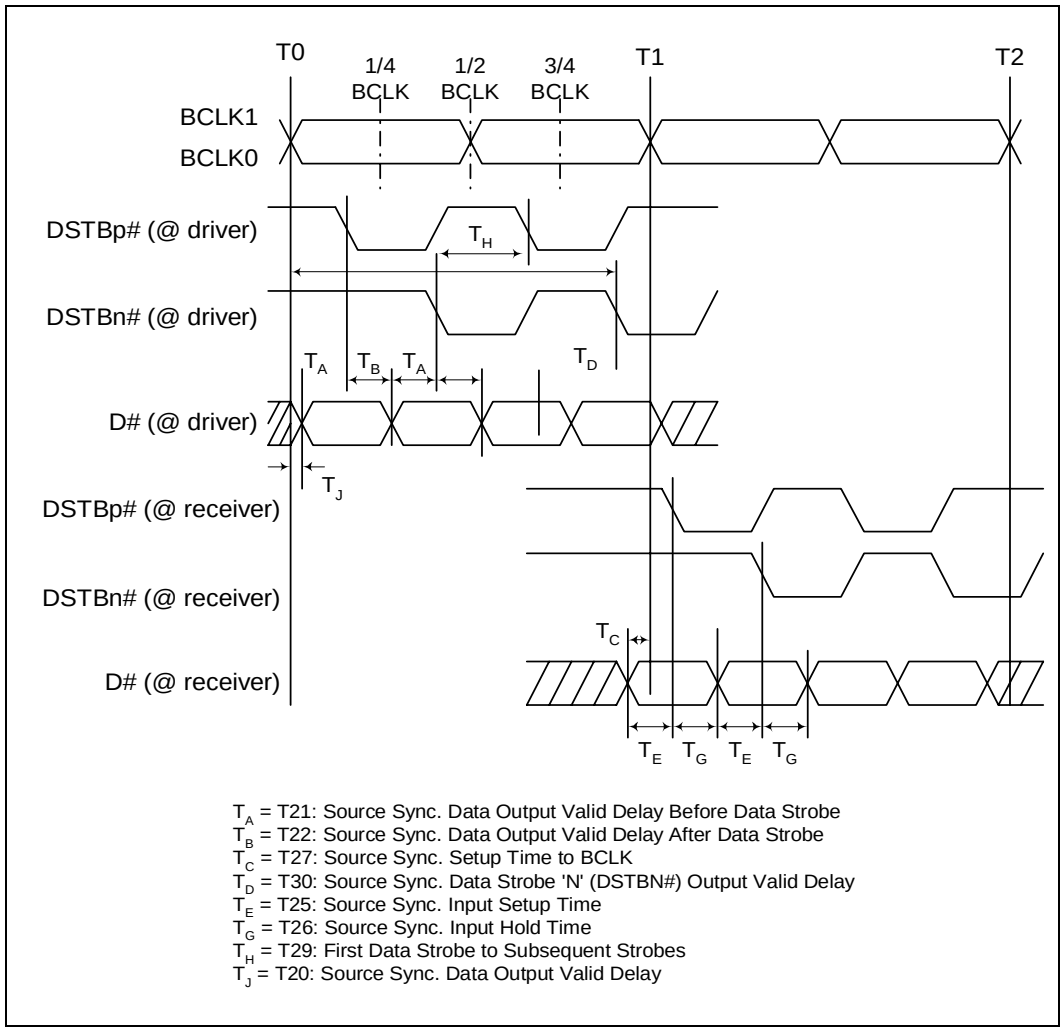
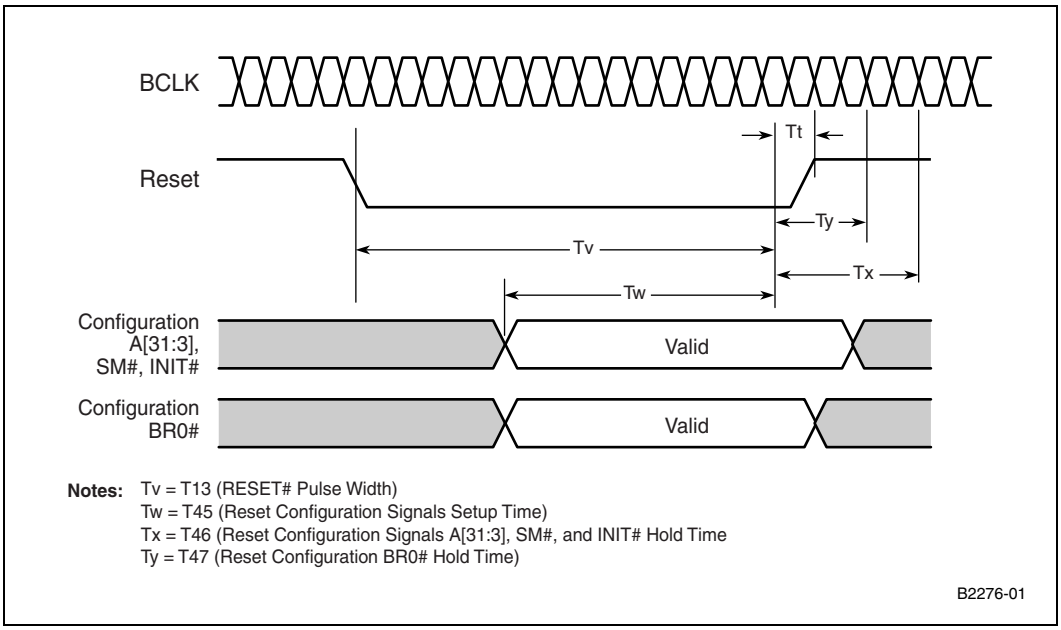


Figure 10. System Bus Source Synchronous 4X (Data) Timing Waveform



T_A = T21: Source Sync. Data Output Valid Delay Before Data Strobe
T_B = T22: Source Sync. Data Output Valid Delay After Data Strobe
T_C = T27: Source Sync. Setup Time to BCLK
T_D = T30: Source Sync. Data Strobe 'N' (DSTBN#) Output Valid Delay
T_E = T25: Source Sync. Input Setup Time
T_G = T26: Source Sync. Input Hold Time
T_H = T29: First Data Strobe to Subsequent Strobes
T_J = T20: Source Sync. Data Output Valid Delay

Figure 11. System Bus Reset and Configuration Timing Waveform



Notes: Tv = T13 (RESET# Pulse Width)
Tw = T45 (Reset Configuration Signals Setup Time)
Tx = T46 (Reset Configuration Signals A[31:3], SM#, and INIT# Hold Time
Ty = T47 (Reset Configuration BR0# Hold Time)

B2276-01

Figure 12. Power-On Reset and Configuration Timing Waveform

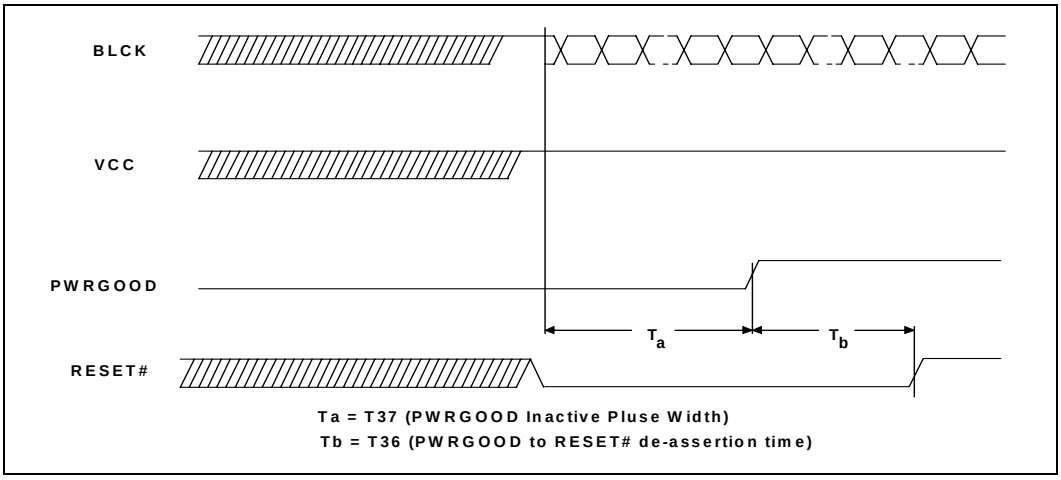


Figure 13. TAP Valid Delay Timing Waveform

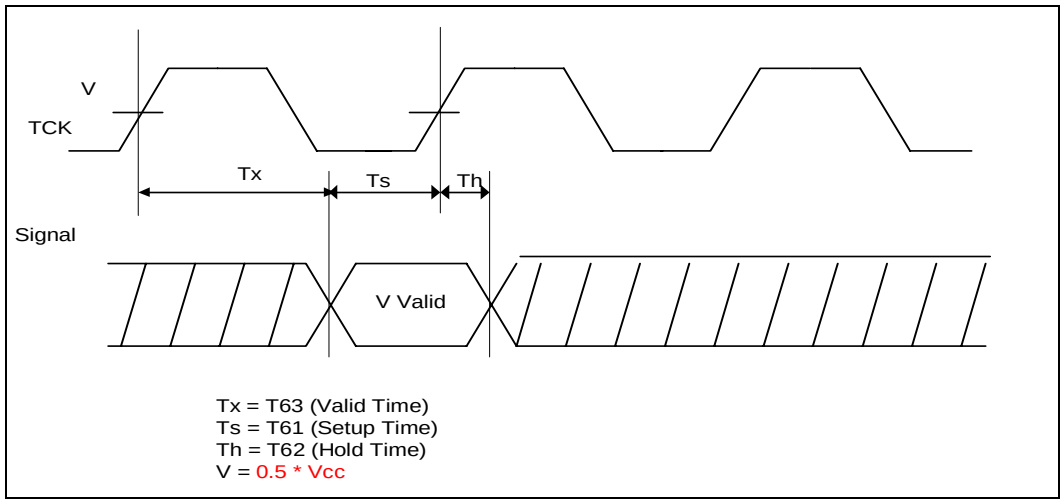


Figure 14. Test Reset (TRST#), Async GTL+ Input, and PROCHOT# Timing Waveform

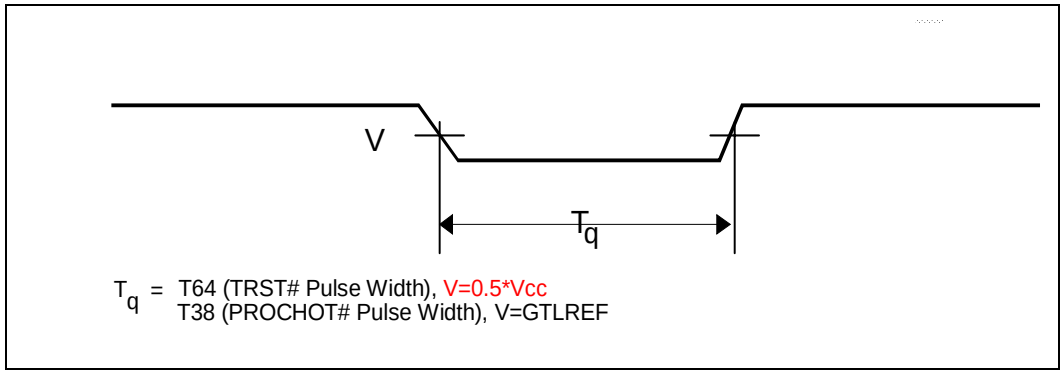


Figure 15. THERMTRIP# to V_{CC} Timing

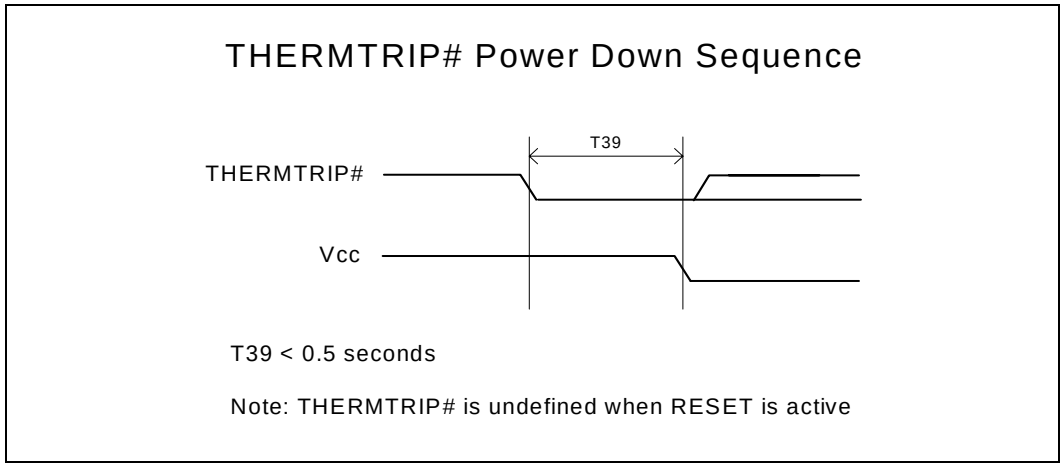
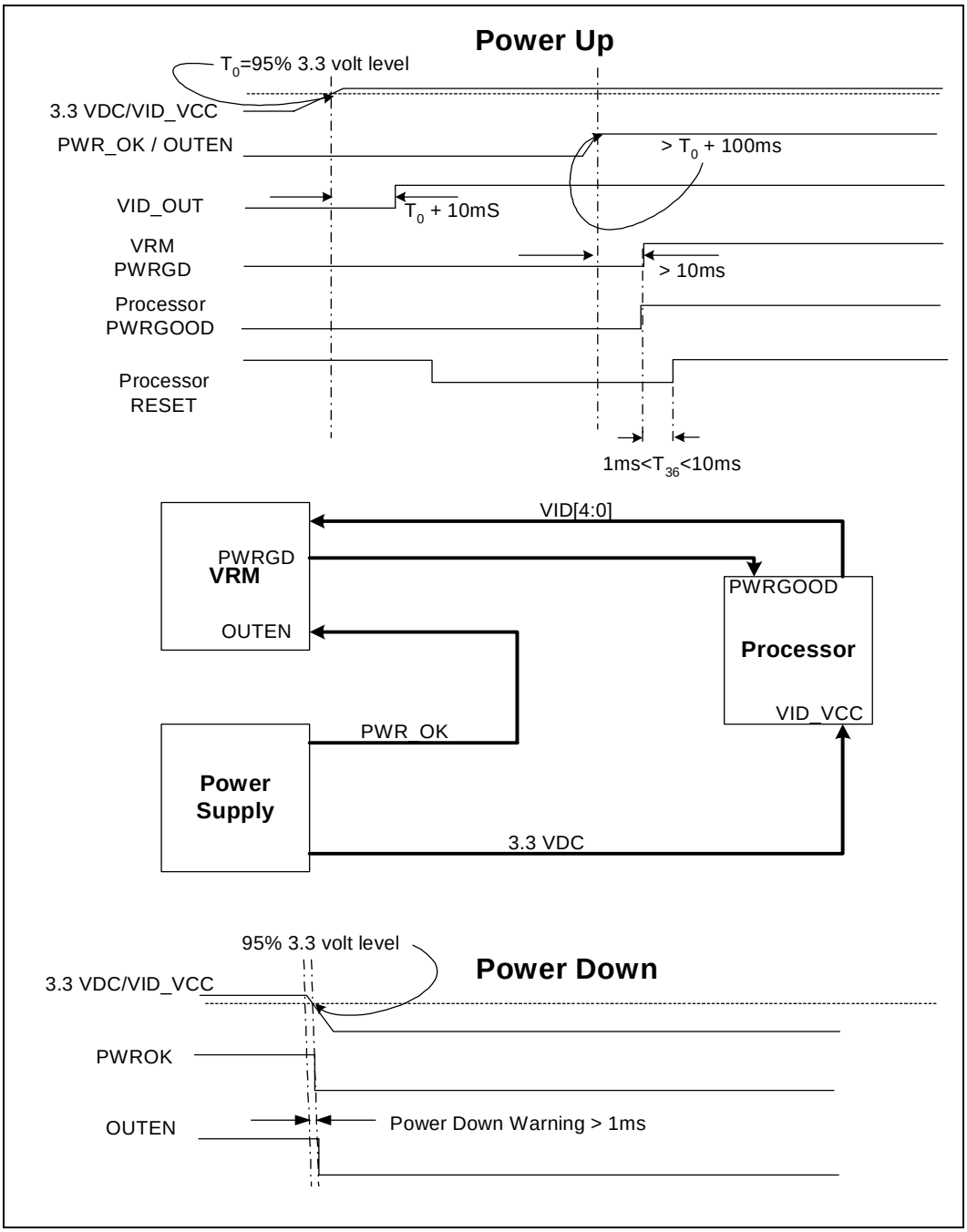


Figure 16. Example 3.3 VDC/VID_V_{CC} Sequencing



3.0 System Bus Signal Quality Specifications

This section documents signal quality metrics used to derive topology and routing guidelines through simulation. All specifications are made at the processor core (pad measurements).

Source synchronous data transfer requires the clean reception of data signals and their associated strobes. Ringing below receiver thresholds, non-monotonic signal edges, and excessive voltage swing may adversely affect system timings. Ringback and signal non-monotinicity cannot be tolerated since these phenomena may inadvertently advance receiver state machines. Excessive signal swings (overshoot and undershoot) are detrimental to silicon gate oxide integrity, and may cause device failure when absolute voltage limits are exceeded. Additionally, overshoot and undershoot may degrade timing due to the build up of inter-symbol interference (ISI) effects. For these reasons, it is crucial that the designer assure acceptable signal quality across all systematic variations encountered in volume manufacturing.

Specifications for signal quality are for measurements at the processor core only and are only observable through simulation. The same is true for all system bus AC timing specifications in Section 2.13. Therefore, proper simulation of the processor system bus is the only means to verify proper timing and signal quality metrics.

3.1 System Bus Clock (BCLK) Signal Quality Specifications and Measurement Guidelines

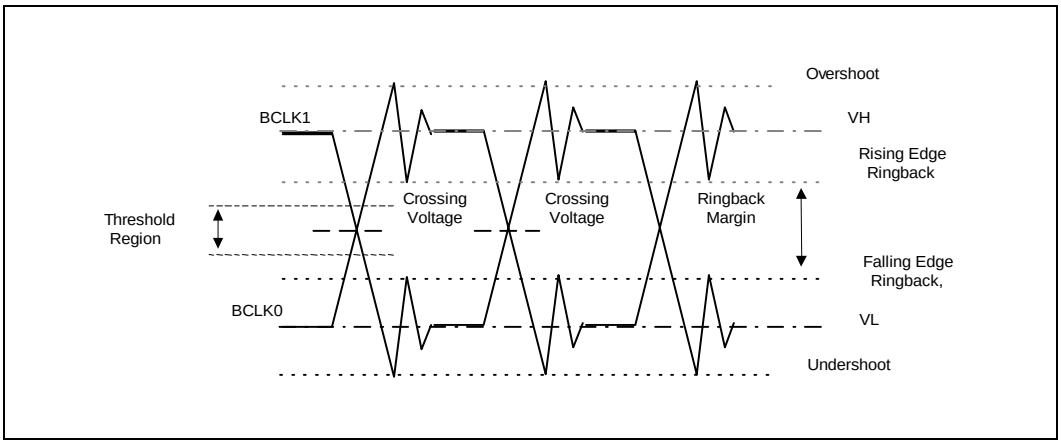
Table 19 describes the signal quality specifications at the processor pads for the processor system bus clock (BCLK) signals. Figure 17 describes the signal quality waveform for the system bus clock at the processor pads.

Table 19. BCLK Signal Quality Specifications

Parameter	Min	Max	Unit	Figure	Notes
BCLK[1:0] Overshoot	N/A	0.30	V	17	
BCLK[1:0] Undershoot	N/A	0.30	V	17	
BCLK[1:0] Ringback Margin	0.20	N/A	V	17	
BCLK[1:0] Threshold Region	N/A	0.10	V	17	†

† The rising and falling edge ringback voltage specified is the minimum (rising) or maximum (falling) absolute voltage the BCLK signal may dip back to after passing the V_{IH} (rising) or V_{IL} (falling) voltage limits. This specification is an absolute value.

Figure 17. BCLK[1:0] Signal Integrity Waveform



3.2 System Bus Signal Quality Specifications and Measurement Guidelines

Many scenarios have been simulated to generate a set of AGTL+ layout guidelines which are available in the appropriate platform design guidelines.

Table 20 provides the signal quality specifications for all processor signals for use in simulating signal quality at the processor pads.

Maximum allowable overshoot and undershoot specifications for a given duration of time are detailed in Table 22 through Table 25. Figure 18 shows the system bus ringback tolerance for low-to-high transitions and Figure 19 shows ringback tolerance for high-to-low transitions.

Table 20. Ringback Specifications for AGTL+ and Asynchronous GTL+ Buffers

Signal Group	Transition	Maximum Ringback (with Input Diodes Present)	Unit	Figure	Notes
AGTL+, Asynch GTL+	L → H	GTLREF + 0.100*GTLREF	V	18	1, 2, 3, 4, 5, 6
AGTL+, Asynch GTL+	H → L	GTLREF - 0.100*GTLREF	V	19	1, 2, 3, 4, 5, 6

NOTES:
1. All signal integrity specifications are measured at the processor core (pads).
2. Specifications are for the edge rate of 0.3 - 4.0 V/ns at the receiver.
3. All values specified by design characterization.
4. Please see Section 3.0 for maximum allowable overshoot.
5. Ringback between GTLREF + 100 mV and GTLREF - 100 mV is not supported.
6. Intel recommends simulations not exceed a ringback value of GTLREF ± 200 mV to allow margin for other sources of system noise.

Table 21. Ringback Specifications for TAP Buffers

Signal Group	Transition	Maximum Ringback (with Input Diodes Present)	Threshold	Unit	Figure	Notes
TAP and PWRGOOD	L → H	$V_{T+(max)}$ TO $V_{T-(max)}$	$V_{T+(max)}$	V	20	1, 2, 3, 4
TAP and PWRGOOD	H → L	$V_{T-(min)}$ TO $V_{T+(min)}$	$V_{T-(min)}$	V	21	1, 2, 3, 4

NOTES:
1. All signal integrity specifications are measured at the processor core (pads).
2. Specifications are for the edge rate of 0.3 - 4.0 V/ns.
3. All values specified by design characterization.
4. Please see Section 3.3 for maximum allowable overshoot.

Figure 18. Low-to-High System Bus Receiver Ringback Tolerance for AGTL+ and Asynchronous GTL+ Buffers

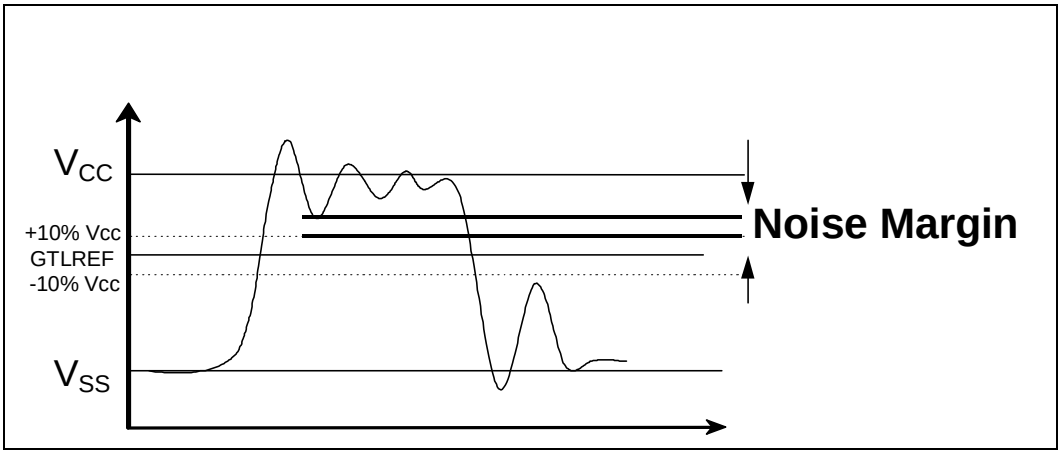


Figure 19. High-to-Low System Bus Receiver Ringback Tolerance for AGTL+ and Asynchronous GTL+ Buffers

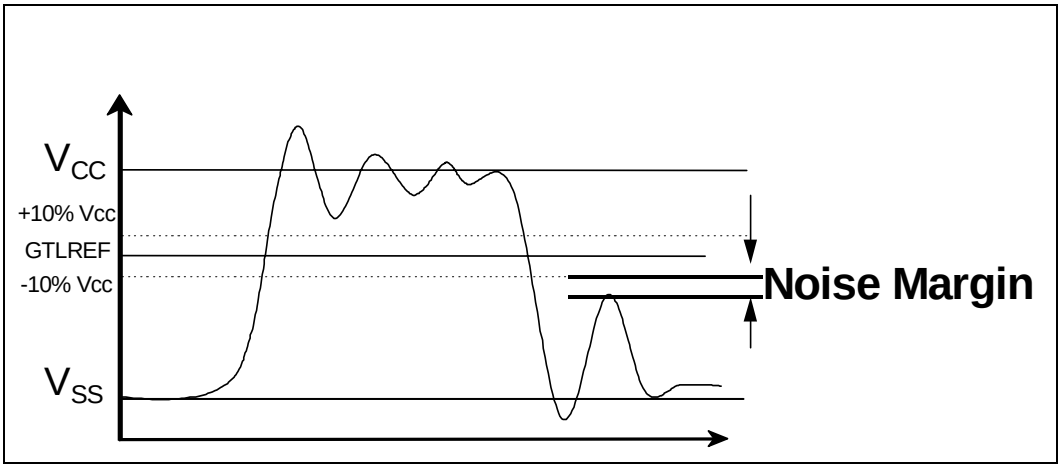


Figure 20. Low-to-High System Bus Receiver Ringback Tolerance for PWRGOOD TAP Buffers

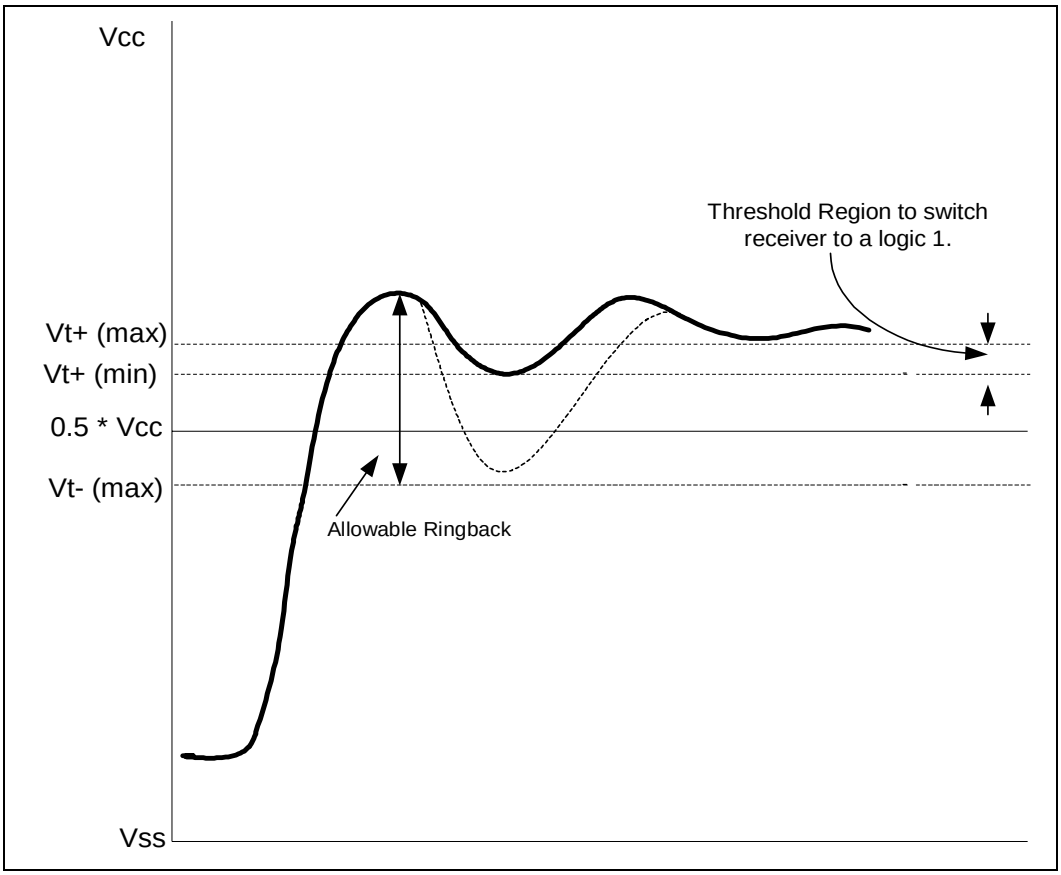
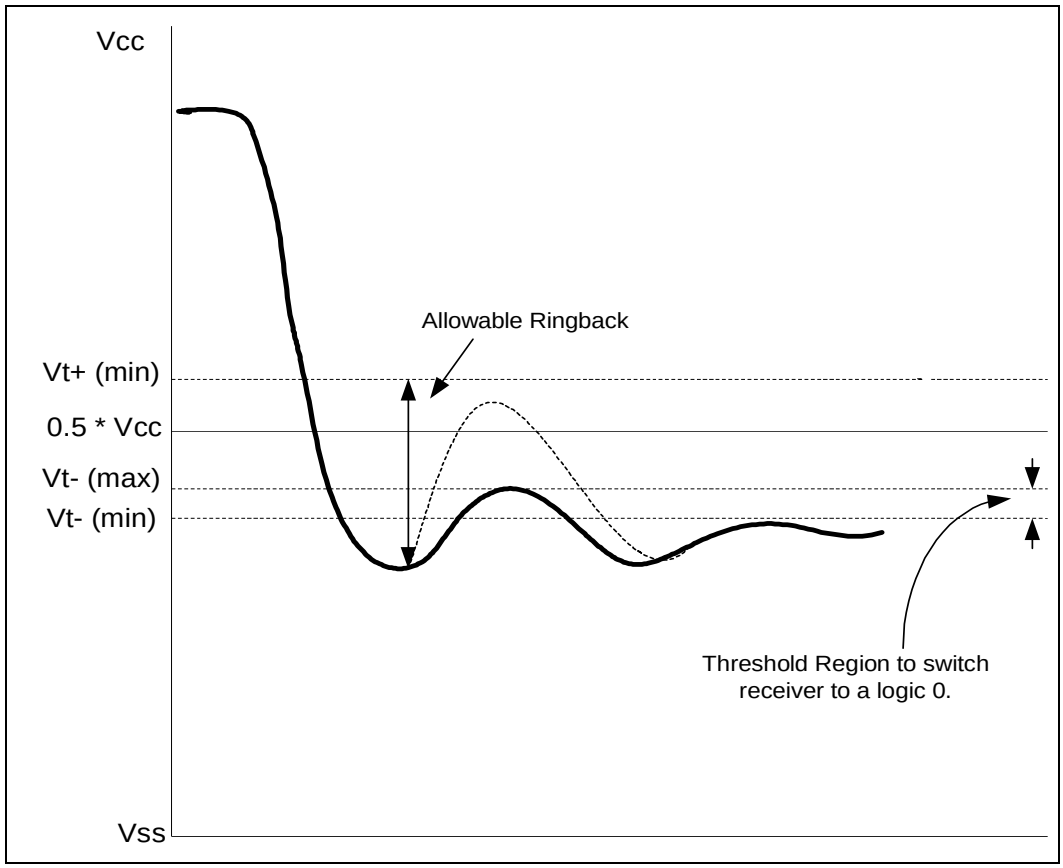


Figure 21. High-to-Low System Bus Receiver Ringback Tolerance for PWRGOOD and TAP Buffer



3.3 System Bus Signal Quality Specifications and Measurement Guidelines

3.3.1 Overshoot/Undershoot Guidelines

Overshoot (or undershoot) is the absolute value of the maximum voltage above or below V_{SS}. The overshoot/undershoot specifications limit transitions beyond V_{CC} or V_{SS} due to the fast signal edge rates. The processor may be damaged by single and/or repeated overshoot or undershoot events on any input, output, or I/O buffer when the charge is large enough (i.e., when the over/undershoot is great enough). Determining the impact of an overshoot/undershoot condition requires knowledge of the magnitude, the pulse direction, and the activity factor (AF). Permanent damage to the processor is the likely result of excessive overshoot/undershoot.

When performing simulations to determine impact of overshoot and undershoot, ESD diodes must be properly characterized. ESD protection diodes do not act as voltage clamps and may not provide overshoot or undershoot protection. ESD diodes modelled within Intel's signal integrity models do not clamp undershoot or overshoot and may yield correct simulation results. When other signal integrity models are being used to characterize the processor system bus, care must be taken to

ensure that ESD models do not clamp extreme voltage levels. Intel's signal integrity models also contain I/O capacitance characterization. Therefore, removing the ESD diodes from a signal integrity model may impact results and may yield excessive overshoot/undershoot.

3.3.2 Overshoot/Undershoot Magnitude

Magnitude describes the maximum potential difference between a signal and its voltage reference level (V_{SS}). It is important to note that overshoot and undershoot conditions are separate and their impact must be determined independently.

Overshoot/undershoot magnitude levels must observe the absolute maximum specifications listed in Table 22 through Table 25. These specifications must not be violated at any time regardless of bus activity or system state. Within these specifications are threshold levels that define different allowed pulse duration. Provided that the magnitude of the overshoot/undershoot is within the absolute maximum specifications, the pulse magnitude, duration and activity factor must all be used to determine when the overshoot/undershoot pulse is within specifications.

3.3.3 Overshoot/Undershoot Pulse Duration

Pulse duration describes the total time an overshoot/undershoot event exceeds the overshoot/undershoot reference voltage (V_{CC}). The total time could encompass several oscillations above the reference voltage. Multiple overshoot/undershoot pulses within a single overshoot/undershoot event may need to be measured to determine the total pulse duration.

Note: Oscillations below the reference voltage cannot be subtracted from the total overshoot/undershoot pulse duration.

3.3.4 Activity Factor

Activity Factor (AF) describes the frequency of overshoot (or undershoot) occurrence relative to a clock. Since the highest frequency of assertion of any common clock signal is every other clock, an AF = 1 indicates that the specific overshoot (or undershoot) waveform occurs every other clock cycle. Thus, an AF = 0.01 indicates that the specific overshoot (or undershoot) waveform occurs one time in every 200 clock cycles.

For source synchronous signals (address, data, and associated strobes), the activity factor is in reference to the strobe edge. The highest frequency of assertion of any source synchronous signal is every active edge of its associated strobe. So, an AF = 1 indicates that the specific overshoot (or undershoot) waveform occurs every strobe cycle.

The specifications provided in Table 22 through Table 25 show the maximum pulse duration allowed for a given overshoot/undershoot magnitude at a specific activity factor. Each table entry is independent of all others, meaning that the pulse duration reflects the existence of overshoot/undershoot events of that magnitude ONLY. A platform with an overshoot/undershoot that just meets the pulse duration for a specific magnitude where the AF < 1, means that there may be no other overshoot/undershoot events, even of lesser magnitude (note that when AF = 1, the event occurs at all times and no other events may occur).

Note: The following three notes apply to the activity factor.

1. Activity factor for common clock AGTL+ signals is referenced to BCLK[1:0] frequency.
2. Activity factor for source synchronous (2x) signals is referenced to ADSTB[1:0]#.
3. Activity factor for source synchronous (4x) signals is referenced to DSTBP[3:0]#and DSTBN[3:0]#.

3.3.5 Reading Overshoot/Undershoot Specification Tables

The processor overshoot/undershoot specification is not a simple single value. Instead, many factors are needed to determine what the overshoot/undershoot specification is. In addition to the magnitude of the overshoot, the following parameters must also be known: the width of the overshoot and the activity factor (AF). To determine the allowed overshoot for a particular overshoot event, the following must be done:

1. Determine the *signal group* that particular signal falls into. For AGTL+ signals operating in the 4X source synchronous domain, Table 22 should be used. For AGTL+ signals operating in the 2X source synchronous domain, Table 23 should be used. When the signal is an AGTL+ signal operating in the common clock domain, Table 24 should be used. Finally, for all other signals residing in the 33 MHz domain (asynchronous GTL+, TAP, etc.), Table 25 should be used.
2. Determine the *magnitude* of the overshoot or the undershoot (relative to V_{SS}).
3. Determine the *activity factor* (how often does this overshoot occurs).
4. Next, from the appropriate specification table, determine the *maximum pulse duration* (in nanoseconds) allowed.
5. Compare the specified maximum pulse duration to the signal being measured. When the pulse duration measured is less than the pulse duration shown in the table, the signal meets the specifications.

Undershoot events must be analyzed separately from overshoot events as they are mutually exclusive.

3.3.6 Determining When a System Meets the Overshoot/Undershoot Specifications

The overshoot/undershoot specifications listed in the following tables specify the allowable overshoot/undershoot for a single overshoot/undershoot event. However most systems may have multiple overshoot and/or undershoot events that each have their own set of parameters (duration, AF and magnitude). While each overshoot on its own may meet the overshoot specification, when the total impact of all overshoot events are considered, the system may fail. A guideline to ensure a system passes the overshoot and undershoot specifications is presented as follows:

- Ensure that no signal ever exceeds V_{CC} or -0.25 V *OR*
- When only one overshoot/undershoot event magnitude occurs, ensure it meets the overshoot/ undershoot specifications in the following tables *OR*
- When multiple overshoots and/or multiple undershoots occur, measure the worst case pulse duration for each magnitude and compare the results against the AF = 1 specifications. When all of these worst case overshoot or undershoot events meet the specifications (measured time < specifications) in the table (where AF=1), the system passes.

The following notes apply to Table 22 through Table 25:

- Absolute Maximum Overshoot magnitude of 1.8 V must never be exceeded.
- Absolute Maximum Overshoot is measured referenced to V_{SS}, Pulse Duration of overshoot is measured relative to V_{CC}.
- Absolute Maximum Undershoot and Pulse Duration of undershoot is measured relative to V_{SS}.
- Ringback below V_{CC} cannot be subtracted from overshoots/undershoots.
- Lesser undershoot does not allocate longer or larger overshoot.
- System designers are strongly encouraged to follow Intel's layout guidelines.
- All values specified by design characterization.

Table 22. Source Synchronous (400 MHz) AGTL+ Signal Group Overshoot/Undershoot Tolerance

Absolute Maximum Overshoot (V)	Absolute Maximum Undershoot (V)	Pulse Duration (ns) AF = 1	Pulse Duration (ns) AF = 0.1	Pulse Duration (ns) AF = 0.01
1.70	-0.40	0.42	4.18	5.00
1.65	-0.35	1.25	5.00	5.00
1.60	-0.30	3.66	5.00	5.00
1.55	-0.25	5.00	5.00	5.00
1.50	-0.20	5.00	5.00	5.00
1.45	-0.15	5.00	5.00	5.00
1.40	-0.10	5.00	5.00	5.00
1.35	-0.05	5.00	5.00	5.00

NOTES:
1. These specifications are measured at the processor pad.
2. Assumes a BCLK period of 10 ns.
3. AF is referenced to associated source synchronous strobes

Table 23. Source Synchronous (400 MHz) AGTL+ Signal Group Overshoot/Undershoot Tolerance

Absolute Maximum Overshoot (V)	Absolute Maximum Undershoot (V)	Pulse Duration (ns) AF = 1	Pulse Duration (ns) AF = 0.1	Pulse Duration (ns) AF = 0.01
1.70	-0.40	0.84	8.36	10.00
1.65	-0.35	2.50	10.00	10.00
1.60	-0.30	7.32	10.00	10.00
1.55	-0.25	10.00	10.00	10.00
1.50	-0.20	10.00	10.00	10.00

NOTES:
1. These specifications are measured at the processor pad.
2. Assumes a BCLK period of 10 ns.
3. AF is referenced to associated source synchronous strobes.

Table 23. Source Synchronous (400 MHz) AGTL+ Signal Group Overshoot/Undershoot Tolerance

Absolute Maximum Overshoot (V)	Absolute Maximum Undershoot (V)	Pulse Duration (ns) AF = 1	Pulse Duration (ns) AF = 0.1	Pulse Duration (ns) AF = 0.01
1.45	-0.15	10.00	10.00	10.00
1.40	-0.10	10.00	10.00	10.00
1.35	-0.05	10.00	10.00	10.00

NOTES:
1. These specifications are measured at the processor pad.
2. Assumes a BCLK period of 10 ns.
3. AF is referenced to associated source synchronous strobes.

Table 24. Common Clock (400 MHz) AGTL+ Signal Group Overshoot/Undershoot Tolerance

Absolute Maximum Overshoot (V)	Absolute Maximum Undershoot (V)	Pulse Duration (ns) AF = 1	Pulse Duration (ns) AF = 0.1	Pulse Duration (ns) AF = 0.01
1.70	-0.40	1.68	16.72	20.00
1.65	-0.35	5.00	20.00	20.00
1.60	-0.30	14.64	20.00	20.00
1.55	-0.25	20.00	20.00	20.00
1.50	-0.20	20.00	20.00	20.00
1.45	-0.15	20.00	20.00	20.00
1.40	-0.10	20.00	20.00	20.00
1.35	-0.05	20.00	20.00	20.00

NOTES:
1. These specifications are measured at the processor pad.
2. BCLK period is 10 ns.
3. WIRED OR processor signals may tolerate up to 1 V of overshoot/undershoot.
4. AF is referenced to BCLK[1:0]

Table 25. 400 MHz Asynchronous GTL+, PWRGOOD, and TAP Signal Groups Overshoot/Undershoot Tolerance (Sheet 1 of 2)

Absolute Maximum Overshoot (V)	Absolute Maximum Undershoot (V)	Pulse Duration (ns) AF = 1	Pulse Duration (ns) AF = 0.1	Pulse Duration (ns) AF = 0.01
1.70	-0.40	5.04	50.16	60.00
1.65	-0.35	14.99	60.00	60.00
1.60	-0.30	43.92	60.00	60.00
1.55	-0.25	60.00	60.00	60.00
1.50	-0.20	60.00	60.00	60.00

NOTES:
1. These specifications are measured at the processor pad.
2. These signals are assumed in a 33 MHz time domain.

Table 25. 400 MHz Asynchronous GTL+, PWRGOOD, and TAP Signal Groups Overshoot/Undershoot Tolerance (Sheet 2 of 2)

Absolute Maximum Overshoot (V)	Absolute Maximum Undershoot (V)	Pulse Duration (ns) AF = 1	Pulse Duration (ns) AF = 0.1	Pulse Duration (ns) AF = 0.01
1.45	-0.15	60.00	60.00	60.00
1.40	-0.10	60.00	60.00	60.00
1.35	-0.05	60.00	60.00	60.00

NOTES:
1. These specifications are measured at the processor pad.
2. These signals are assumed in a 33 MHz time domain.

Table 26. Source Synchronous (533 MHz) AGTL+ Signal Group Overshoot/Undershoot Tolerance

Absolute Maximum Overshoot(V)	Absolute Maximum Undershoot (V)	Pulse Duration (ns) AF=1	Pulse Duration (ns) AF-0.1	Pulse Duration (ns) AF=0.01
1.700	-0.400	0.32	3.14	3.75
1.650	-0.350	0.94	3.75	3.75
1.600	-0.300	2.74	3.75	3.75
1.550	-0.250	3.75	3.75	3.75
1.500	-0.200	3.75	3.75	3.75
1.450	-0.150	3.75	3.75	3.75
1.400	-0.100	3.75	3.75	3.75
1.350	-0.050	3.75	3.75	3.75

NOTES:
1. These specifications are measured at the processor pad.
2. Assumes a BCLK period of 10 ns.
3. AF is referenced to associated source synchronous strobes

Table 27. Source Synchronous (533 MHz) AGTL+ Signal Group Overshoot/Undershoot Tolerance (Sheet 1 of 2)

Absolute Maximum Overshoot(V)	Absolute Maximum Undershoot (V)	Pulse Duration (ns) AF=1	Pulse Duration (ns) AF-0.1	Pulse Duration (ns) AF=0.01
1.700	-0.400	0.63	6.27	7.50
1.650	-0.350	1.87	7.50	7.50
1.600	-0.300	5.49	7.50	7.50
1.550	-0.250	7.50	7.50	7.50
1.500	-0.200	7.50	7.50	7.50
1.450	-0.150	7.50	7.50	7.50

Table 27. Source Synchronous (533 MHz) AGTL+ Signal Group Overshoot/Undershoot Tolerance (Continued) (Sheet 2 of 2)

Absolute Maximum Overshoot(V)	Absolute Maximum Undershoot (V)	Pulse Duration (ns) AF=1	Pulse Duration (ns) AF-0.1	Pulse Duration (ns) AF=0.01
1.400	-0.100	7.50	7.50	7.50
1.350	-0.050	7.50	7.50	7.50

NOTES:
1. These specifications are measured at the processor pad.
2. Assumes a BCLK period of 10 ns.
3. AF is referenced to associated source synchronous strobes.

Table 28. Common Clock (533 MHz) AGTL+ Signal Group Overshoot/Undershoot Tolerance

Absolute Maximum Overshoot(V)	Absolute Maximum Undershoot (V)	Pulse Duration (ns) AF=1	Pulse Duration (ns) AF-0.1	Pulse Duration (ns) AF=0.01
1.700	-0.400	1.26	12.54	15.00
1.650	-0.350	3.75	15.00	15.00
1.600	-0.300	10.98	15.00	15.00
1.550	-0.250	15.00	15.00	15.00
1.500	-0.200	15.00	15.00	15.00
1.450	-0.150	15.00	15.00	15.00
1.400	-0.100	15.00	15.00	15.00
1.350	-0.050	15.00	15.00	15.00

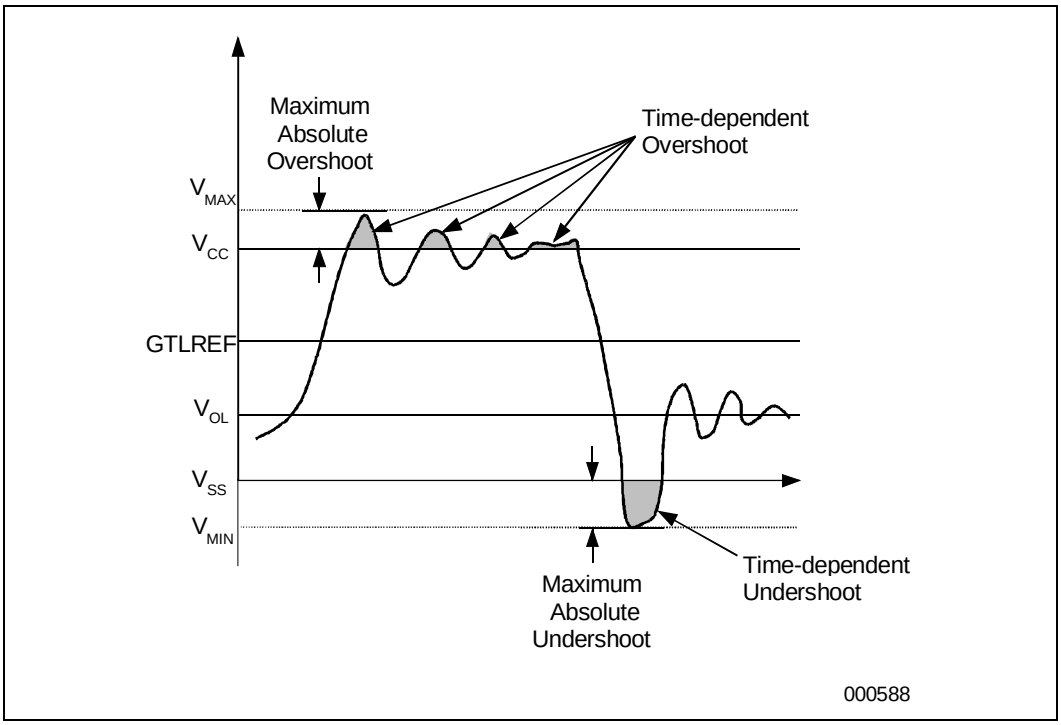
NOTES:
1. These specifications are measured at the processor pad.
2. BCLK period is 10 ns.
3. WIRED OR processor signals may tolerate up to 1 V of overshoot/undershoot.
4. AF is referenced to BCLK[1:0]

Table 29. 533 MHz Asynchronous GTL+, PWRGOOD, and TAP Signal Groups Overshoot/ Undershoot Tolerance

Absolute Maximum Overshoot(V)	Absolute Maximum Undershoot (V)	Pulse Duration (ns) AF=1	Pulse Duration (ns) AF-0.1	Pulse Duration (ns) AF=0.01
1.700	-0.400	3.78	37.62	45.00
1.650	-0.350	11.25	45.00	45.00
1.600	-0.300	32.94	45.00	45.00
1.550	-0.250	45.00	45.00	45.00
1.500	-0.200	45.00	45.00	45.00
1.450	-0.150	45.00	45.00	45.00
1.400	-0.100	45.00	45.00	45.00
1.350	-0.050	45.00	45.00	45.00

NOTES:
1. These specifications are measured at the processor pad.
2. These signals are assumed in a 33 MHz time domain.

Figure 22. Maximum Acceptable Overshoot/Undershoot Waveform



4.0 Mechanical Specifications

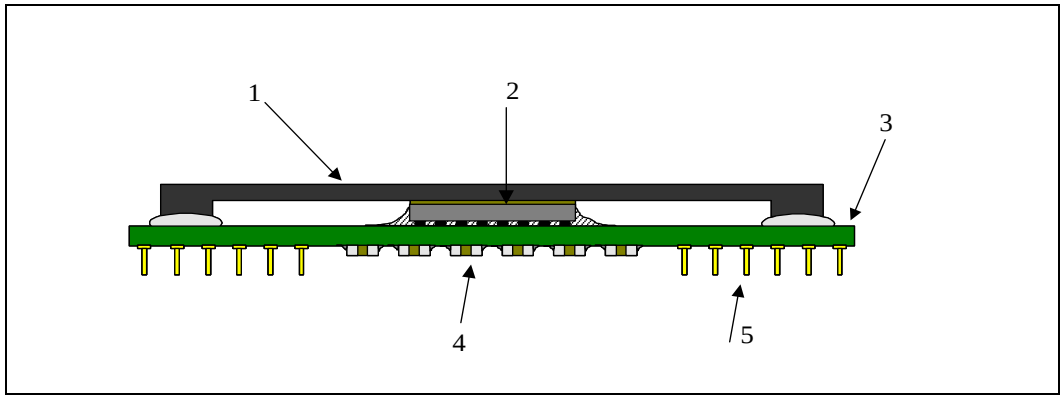
The Low Voltage Intel® Xeon™ processor uses the Flip Chip Micro-Pin Grid Array (FC-µPGA2) package technology. This includes an integrated heat spreader (IHS) mounted to a pinned substrate. Mechanical specifications for the processor are given in this section. See Section 1.1 for terminology definitions. Figure 23 provides a basic assembly drawing and includes the components which make up the entire processor. Package dimensions are provided in Table 30.

The Low Voltage Intel Xeon processor utilizes a surface mount 604-pin zero-insertion force (ZIF) socket for installation into the baseboard. See the *604-Pin Socket Design Guidelines* for further details on the processor socket.

For Figure 25 through Figure 29, the following notes apply:

1. Unless otherwise specified, the following drawings are dimensioned in millimeters.
2. All dimensions are not tested, but are ensured by design characterization.
3. Figures and drawings labelled as “Reference Dimensions” are provided for informational purposes only. Reference Dimensions are extracted from the mechanical design database and are nominal dimensions with no tolerance information applied. Reference Dimensions are NOT checked as part of the processor manufacturing process. Unless noted as such, dimensions in parentheses without tolerances are Reference Dimensions.
4. Drawings are not to scale.

Figure 23. Low Voltage Intel® Xeon™ Processor in the FC-µPGA2 Package: Assembly Drawing



Note: This drawing is not to scale and is for reference only. The assembly applies to the Low Voltage Intel Xeon processor in the FC-µPGA2 package.

1. Integrated Heat Spreader (IHS)
2. Processor die
3. FC-µPGA2 package
4. Land side Capacitors
5. Package Pin

4.1 Mechanical Specifications

Figure 24. Low Voltage Intel® Xeon™ Processor in the FC-µPGA2 Package: Top View-Component Placement Detail

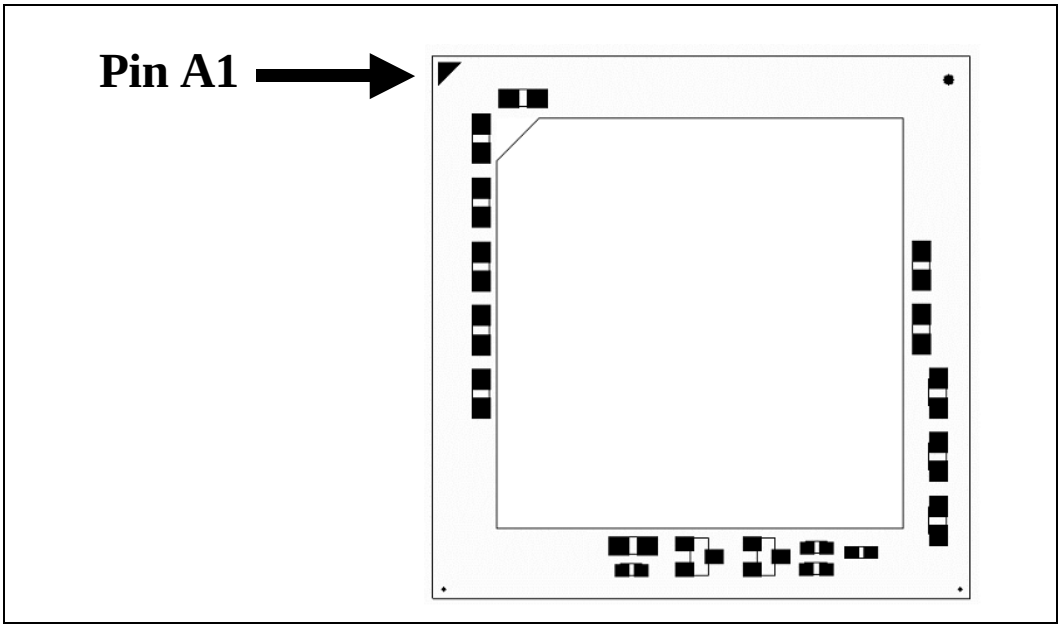


Figure 25. Low Voltage Intel® Xeon™ Processor in the FC-µPGA2 Package: Drawing

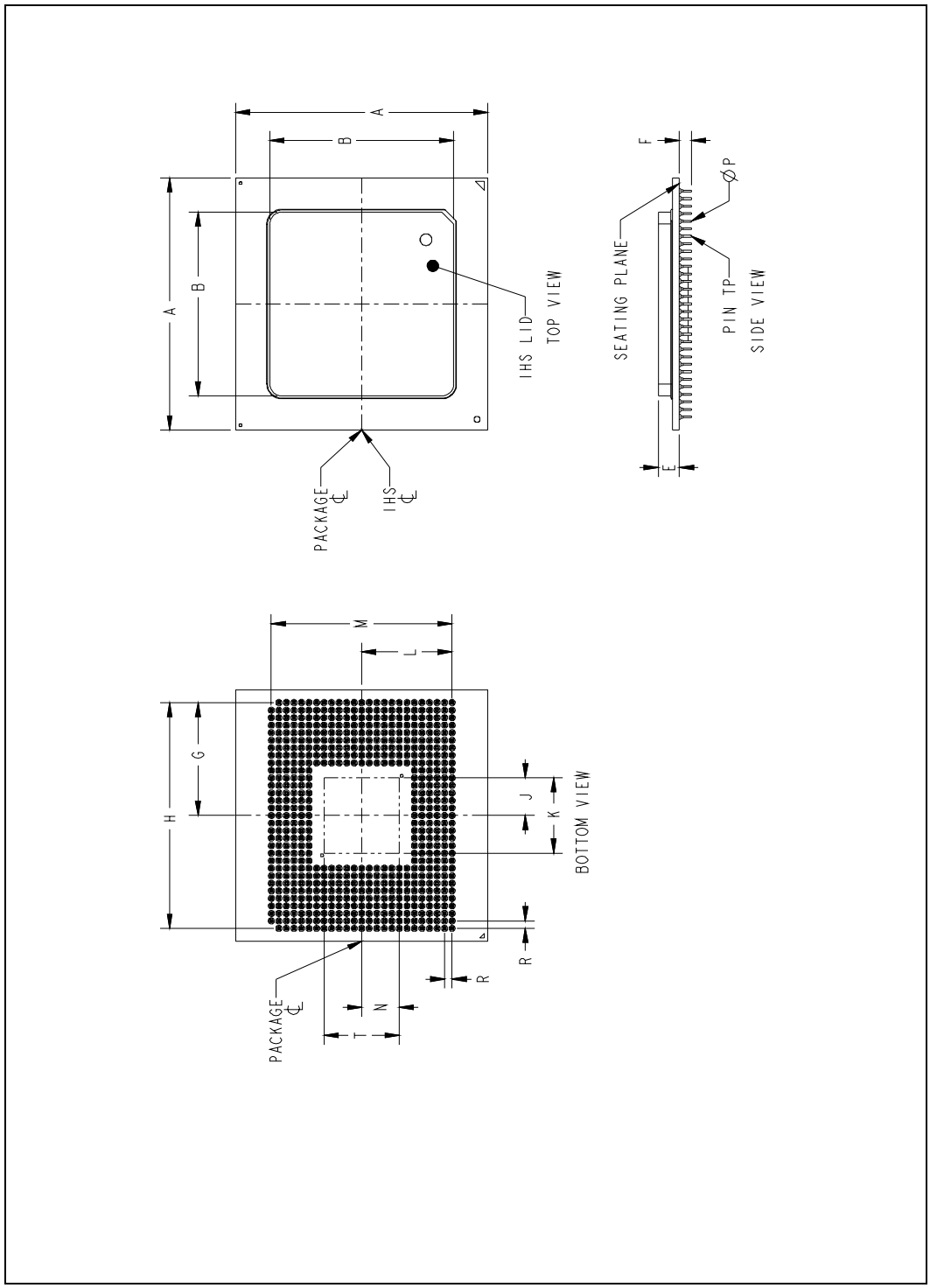


Table 30. Dimensions for the Low Voltage Intel® Xeon™ Processor in the FC-µPGA2 Package

Symbol	Mlimeters			Notes
	Min	Nominal	Max	
A	42.40	42.50	42.60	
B	30.90	31.00	31.10	
E	3.42	3.60	3.78	
F	1.95	2.03	2.11	
G	18.80	19.05	19.30	
H	37.85	38.10	38.35	
J		6.35		Nominal Component Keepin
K		12.70		Nominal Component Keepin
L	14.99	15.24	15.49	
M	30.23	30.48	30.73	
N		6.35		Nominal Component Keepin
R		1.27		Nominal
T		12.70		
ϕP	0.26	0.31	0.36	Pin Diameter
Pin Tp			0.25	

Figure 26 details the keep-in zone for components mounted to the top side of the processor interposer.

Figure 26. Low Voltage Intel® Xeon™ Processor in the FC-µPGA2 Package: Top View-Component Height Keep-In

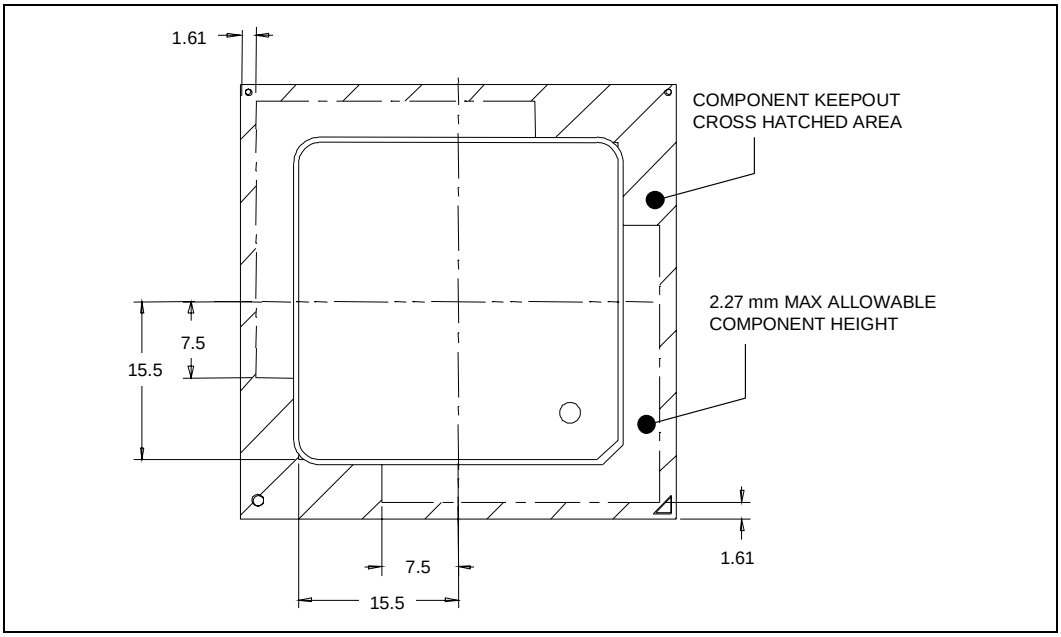


Figure 27. Low Voltage Intel® Xeon™ Processor in the FC-µPGA2 Package: Cross Section View, Pin Side Component Keep-In

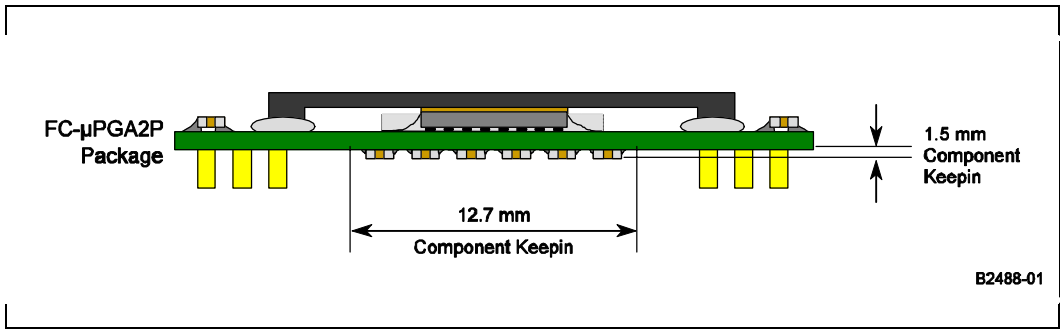


Figure 28. Low Voltage Intel® Xeon™ Processor in the FC-µPGA2 Package: Pin Detail

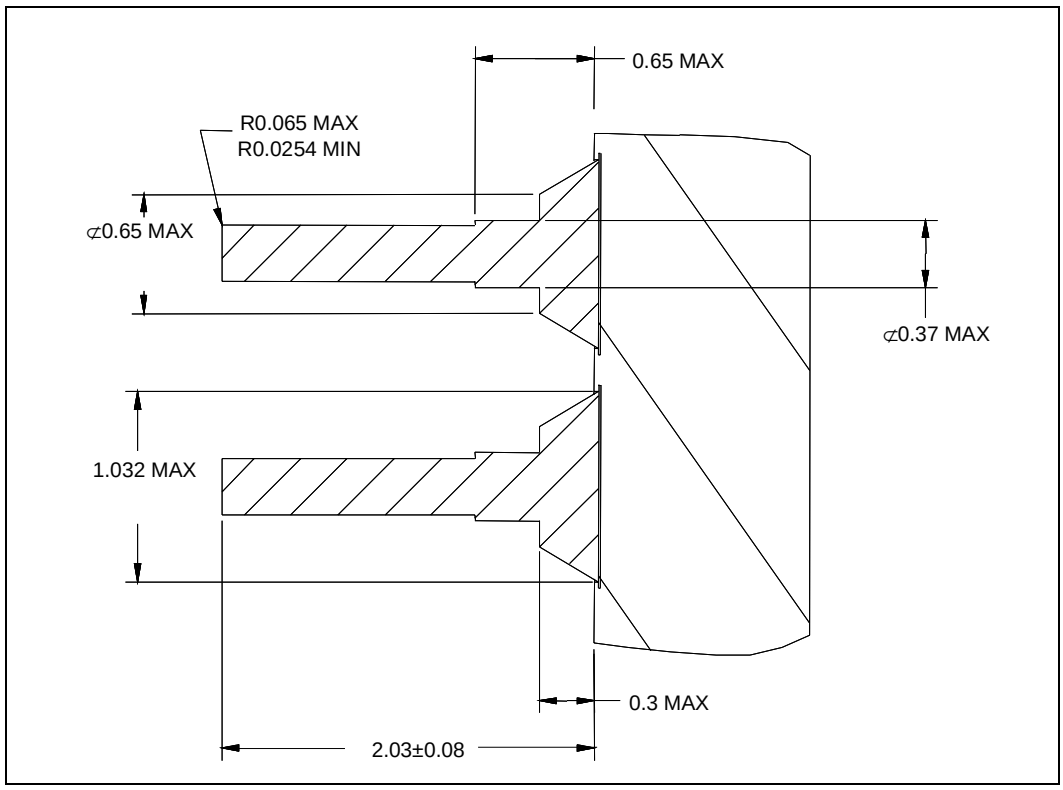
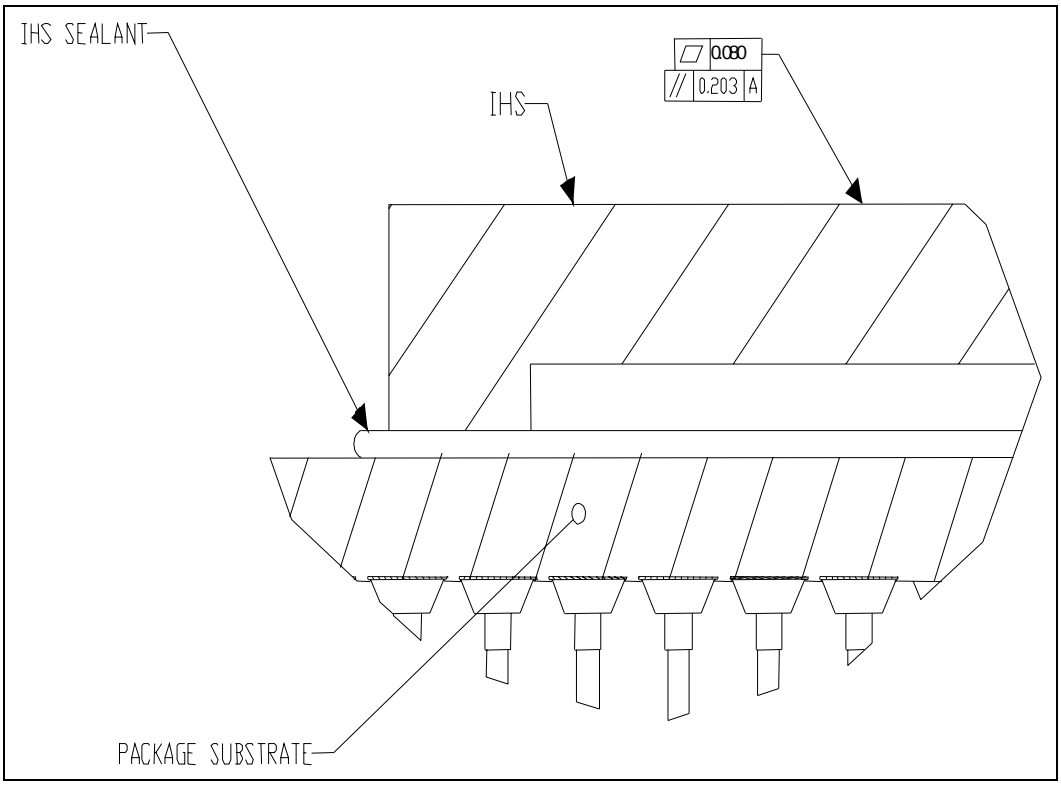


Figure 29 details the flatness and tilt specifications for the IHS of the Low Voltage Intel Xeon processor, respectively. Tilt is measured with the reference datum set to the bottom of the processor interposer.

Figure 29. Low Voltage Intel® Xeon™ Processor FC-µPGA2 Package: IHS Flatness and Tilt Drawing



4.2 Processor Package Load Specifications

Table 31 provides dynamic and static load specifications for the processor IHS. These mechanical load limits should not be exceeded during heat sink assembly, mechanical stress testing, or standard drop and shipping conditions. The heat sink attach solutions must not induce continuous stress onto the processor with the exception of a uniform load to maintain the heat sink-to-processor thermal interface. It is not recommended to use any portion of the processor interposer as a mechanical reference or load bearing surface for thermal solutions.

Table 31. Package Dynamic and Static Load Specifications

Parameter	Max	Unit	Unit
Static	50	lbf	1, 2, 3
Dynamic	50 + 1 lb * 50G input * 1.8 (AF) = 140	lbf	1, 2, 4, 5

NOTES:
1. This specification applies to a uniform compressed load.
2. This is the maximum static force that may be applied by the heatsink and clip to maintain the heatsink and processor interface.
3. These parameters are based on design characterization and not tested.
4. Dynamic loading specifications are defined assuming a maximum duration of 11 ms.
5. The heatsink weight is assumed to be one pound. Shock input to the system during shock testing is assumed to be 50 G's. AF is the amplification factor.

4.3 Insertion Specifications

The processor may be inserted and removed 15 times from a 604-pin socket meeting the *604-Pin Socket Design Guidelines* document. Note that this specification is based on design characterization and is not tested.

4.4 Mass Specifications

Table 32 specifies the processors mass. This includes all components which make up the entire processor product.

Table 32. Processor Mass

Processor	Mass (grams)
The Low Voltage Intel® Xeon™ processor	25

4.5 Materials

The processor is assembled from several components. The basic material properties are described in Table 33.

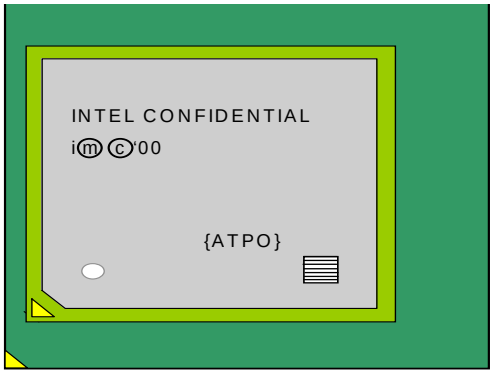
Table 33. Processor Material Properties

Component	Material
Integrated Heat Spreader	Nickel plated copper
FC-µPGA2	BT Resin
Package pins	Cu Alloy 194

4.6 Markings

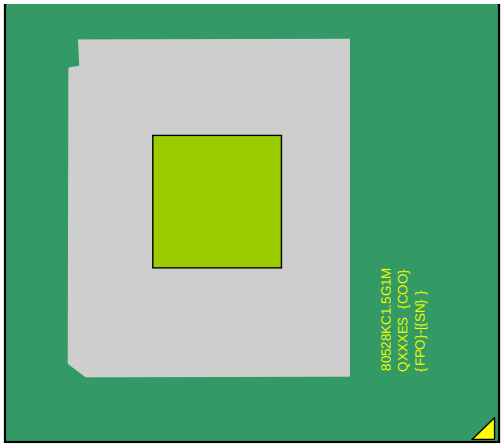
The following section details the processor top-side laser markings. It is provided to aid in the identification of the processor.

Figure 30. Processor Top-Side Markings



NOTES:
1. Character size for laser markings is: height 0.050" (1.27mm), width 0.032" (0.81mm).
2. All characters are in upper case.

Figure 31. Processor Bottom-Side Markings



4.7 Processor Pin-Out Diagram

This section provides two view of the processor pin grid. Figure 32 and Figure 33 detail the coordinates of the processor pins.

Figure 32. Processor Pin Out Diagram: Top View

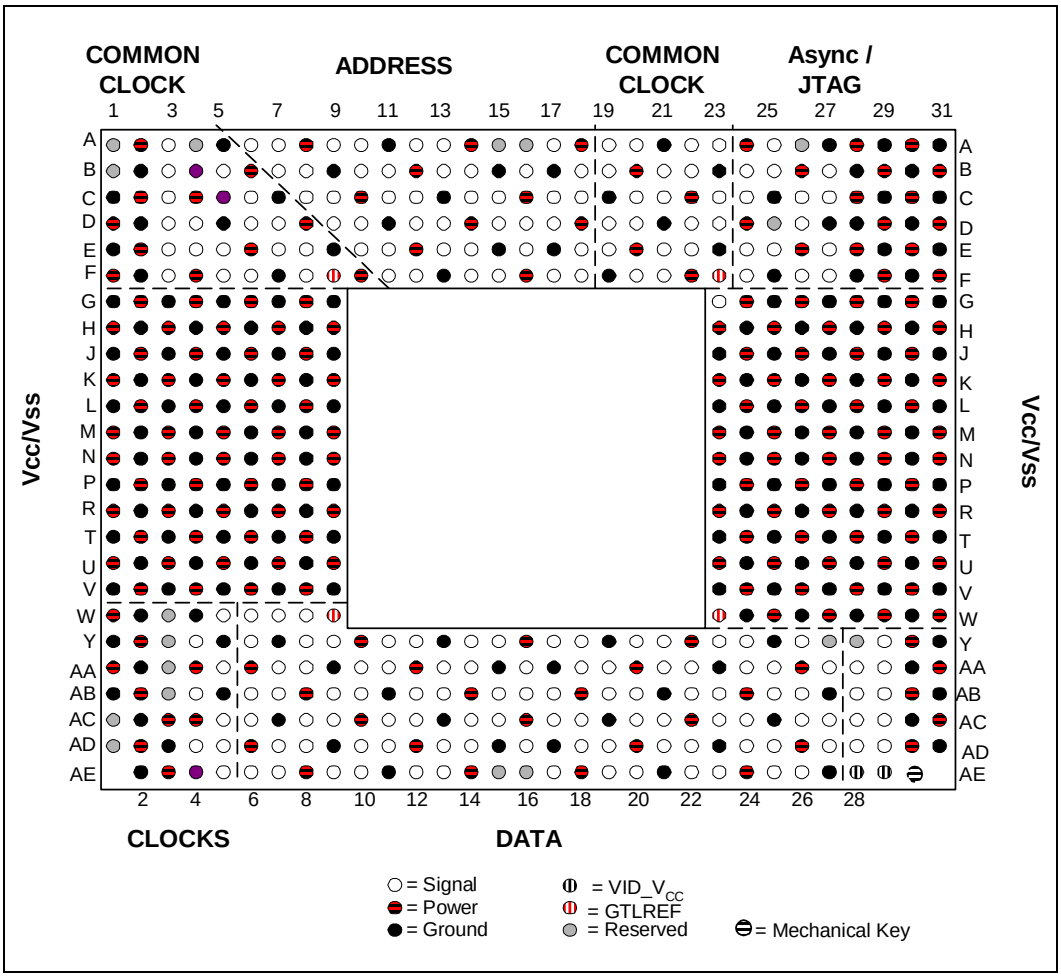
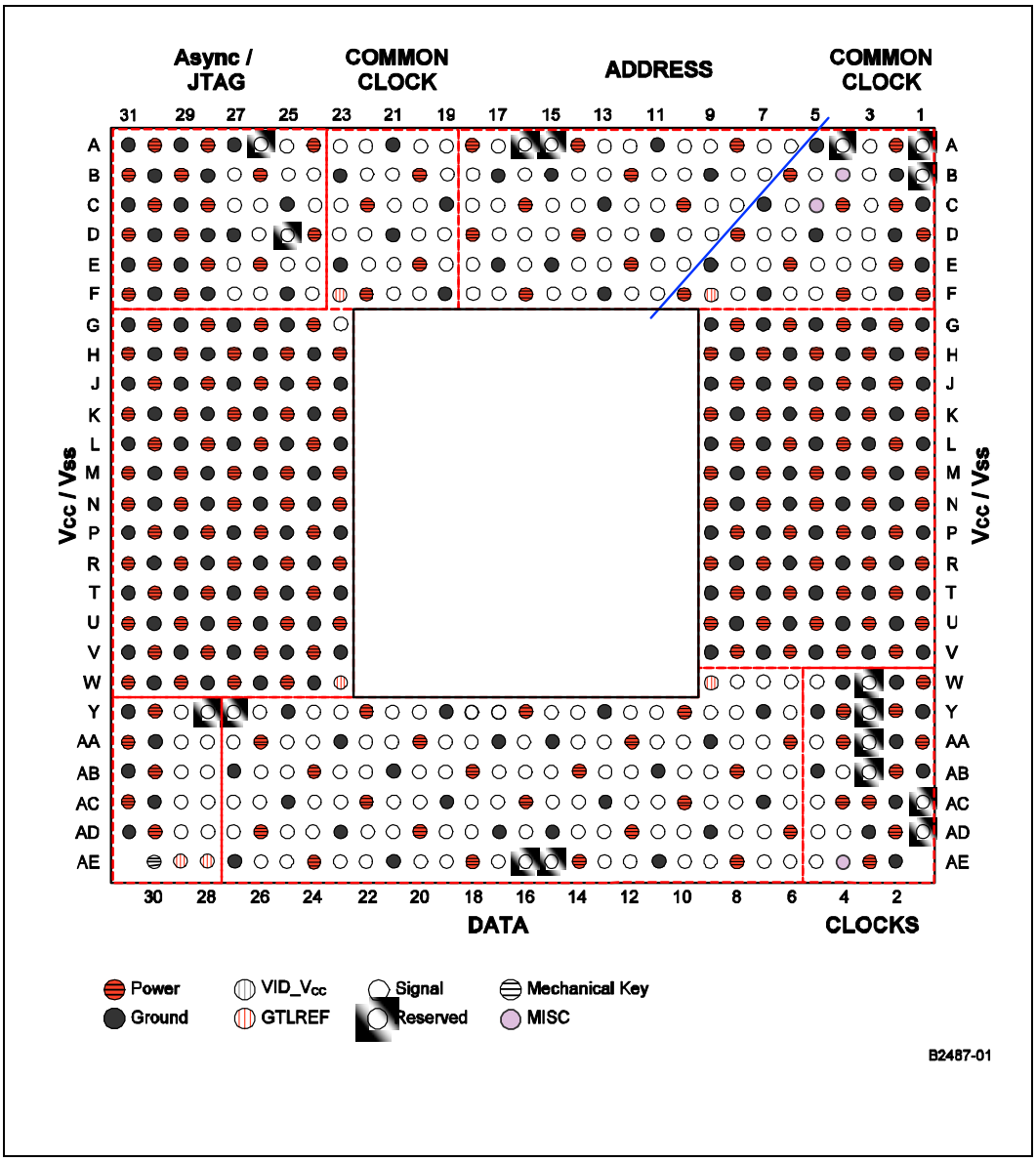


Figure 33. Processor Pin Out Diagram: Bottom View



5.0 Pin Listing and Signal Definitions

5.1 Processor Pin Assignments

Section 2.8 contains the system bus signal groups in Table 5 for the Low Voltage Intel® Xeon™ processor. This section provides a sorted pin list in Table 34 and Table 35. Table 34 is a listing of all processor pins ordered alphabetically by pin name. Table 35 is a listing of all processor pins ordered by pin number.

5.1.1 Pin Listing by Pin Name

Table 34. Pin Listing by Pin Name

Pin Name	Pin No.	Signal Buffer Type	Direction
A3#	A22	Source Sync	Input/Output
A4#	A20	Source Sync	Input/Output
A5#	B18	Source Sync	Input/Output
A6#	C18	Source Sync	Input/Output
A7#	A19	Source Sync	Input/Output
A8#	C17	Source Sync	Input/Output
A9#	D17	Source Sync	Input/Output
A10#	A13	Source Sync	Input/Output
A11#	B16	Source Sync	Input/Output
A12#	B14	Source Sync	Input/Output
A13#	B13	Source Sync	Input/Output
A14#	A12	Source Sync	Input/Output
A15#	C15	Source Sync	Input/Output
A16#	C14	Source Sync	Input/Output
A17#	D16	Source Sync	Input/Output
A18#	D15	Source Sync	Input/Output
A19#	F15	Source Sync	Input/Output
A20#	A10	Source Sync	Input/Output
A21#	B10	Source Sync	Input/Output
A22#	B11	Source Sync	Input/Output
A23#	C12	Source Sync	Input/Output
A24#	E14	Source Sync	Input/Output
A25#	D13	Source Sync	Input/Output
A26#	A9	Source Sync	Input/Output
A27#	B8	Source Sync	Input/Output
A28#	E13	Source Sync	Input/Output

Table 34. Pin Listing by Pin Name

Pin Name	Pin No.	Signal Buffer Type	Direction
A29#	D12	Source Sync	Input/Output
A30#	C11	Source Sync	Input/Output
A31#	B7	Source Sync	Input/Output
A32#	A6	Source Sync	Input/Output
A33#	A7	Source Sync	Input/Output
A34#	C9	Source Sync	Input/Output
A35#	C8	Source Sync	Input/Output
A20M#	F27	Async GTL+	Input
ADS#	D19	Common Clk	Input/Output
ADSTB0#	F17	Source Sync	Input/Output
ADSTB1#	F14	Source Sync	Input/Output
AP0#	E10	Common Clk	Input/Output
AP1#	D9	Common Clk	Input/Output
BCLK0	Y4	Sys Bus Clk	Input
BCLK1	W5	Sys Bus Clk	Input
BINIT#	F11	Common Clk	Input/Output
BNR#	F20	Common Clk	Input/Output
BPM0#	F6	Common Clk	Input/Output
BPM1#	F8	Common Clk	Input/Output
BPM2#	E7	Common Clk	Input/Output
BPM3#	F5	Common Clk	Input/Output

Table 34. Pin Listing by Pin Name

Pin Name	Pin No.	Signal Buffer Type	Direction
BPM4#	E8	Common Clk	Input/Output
BPM5#	E4	Common Clk	Input/Output
BPRI#	D23	Common Clk	Input
BR0#	D20	Common Clk	Input/Output
BR1#	F12	Common Clk	Input
BR2#[1]	E11	Common Clk	Input
BR3#[1]	D10	Common Clk	Input
BSEL0[2]	AA3	Power/Other	Output
BSEL1[2]	AB3	Power/Other	Output
COMP0	AD16	Power/Other	Input
COMP1	E16	Power/Other	Input
D0#	Y26	Source Sync	Input/Output
D1#	AA27	Source Sync	Input/Output
D2#	Y24	Source Sync	Input/Output
D3#	AA25	Source Sync	Input/Output
D4#	AD27	Source Sync	Input/Output
D5#	Y23	Source Sync	Input/Output
D6#	AA24	Source Sync	Input/Output
D7#	AB26	Source Sync	Input/Output
D8#	AB25	Source Sync	Input/Output
D9#	AB23	Source Sync	Input/Output
D10#	AA22	Source Sync	Input/Output
D11#	AA21	Source Sync	Input/Output
D12#	AB20	Source Sync	Input/Output
D13#	AB22	Source Sync	Input/Output
D14#	AB19	Source Sync	Input/Output
D15#	AA19	Source Sync	Input/Output
D16#	AE26	Source Sync	Input/Output
D17#	AC26	Source Sync	Input/Output
D18#	AD25	Source Sync	Input/Output
D19#	AE25	Source Sync	Input/Output
D20#	AC24	Source Sync	Input/Output
D21#	AD24	Source Sync	Input/Output

Table 34. Pin Listing by Pin Name

Pin Name	Pin No.	Signal Buffer Type	Direction
D22#	AE23	Source Sync	Input/Output
D23#	AC23	Source Sync	Input/Output
D24#	AA18	Source Sync	Input/Output
D25#	AC20	Source Sync	Input/Output
D26#	AC21	Source Sync	Input/Output
D27#	AE22	Source Sync	Input/Output
D28#	AE20	Source Sync	Input/Output
D29#	AD21	Source Sync	Input/Output
D30#	AD19	Source Sync	Input/Output
D31#	AB17	Source Sync	Input/Output
D32#	AB16	Source Sync	Input/Output
D33#	AA16	Source Sync	Input/Output
D34#	AC17	Source Sync	Input/Output
D35#	AE13	Source Sync	Input/Output
D36#	AD18	Source Sync	Input/Output
D37#	AB15	Source Sync	Input/Output
D38#	AD13	Source Sync	Input/Output
D39#	AD14	Source Sync	Input/Output
D40#	AD11	Source Sync	Input/Output
D41#	AC12	Source Sync	Input/Output
D42#	AE10	Source Sync	Input/Output
D43#	AC11	Source Sync	Input/Output
D44#	AE9	Source Sync	Input/Output
D45#	AD10	Source Sync	Input/Output
D46#	AD8	Source Sync	Input/Output
D47#	AC9	Source Sync	Input/Output
D48#	AA13	Source Sync	Input/Output
D49#	AA14	Source Sync	Input/Output
D50#	AC14	Source Sync	Input/Output
D51#	AB12	Source Sync	Input/Output
D52#	AB13	Source Sync	Input/Output
D53#	AA11	Source Sync	Input/Output
D54#	AA10	Source Sync	Input/Output
D55#	AB10	Source Sync	Input/Output
D56#	AC8	Source Sync	Input/Output
D57#	AD7	Source Sync	Input/Output
D58#	AE7	Source Sync	Input/Output

Table 34. Pin Listing by Pin Name

Pin Name	Pin No.	Signal Buffer Type	Direction
D59#	AC6	Source Sync	Input/Output
D60#	AC5	Source Sync	Input/Output
D61#	AA8	Source Sync	Input/Output
D62#	Y9	Source Sync	Input/Output
D63#	AB6	Source Sync	Input/Output
DBSY#	F18	Common Clk	Input/Output
DEFER#	C23	Common Clk	Input
DBI0#	AC27	Source Sync	Input/Output
DBI1#	AD22	Source Sync	Input/Output
DBI2#	AE12	Source Sync	Input/Output
DBI3#	AB9	Source Sync	Input/Output
DP0#	AC18	Common Clk	Input/Output
DP1#	AE19	Common Clk	Input/Output
DP2#	AC15	Common Clk	Input/Output
DP3#	AE17	Common Clk	Input/Output
DRDY#	E18	Common Clk	Input/Output
DSTBN0#	Y21	Source Sync	Input/Output
DSTBN1#	Y18	Source Sync	Input/Output
DSTBN2#	Y15	Source Sync	Input/Output
DSTBN3#	Y12	Source Sync	Input/Output
DSTBP0#	Y20	Source Sync	Input/Output
DSTBP1#	Y17	Source Sync	Input/Output
DSTBP2#	Y14	Source Sync	Input/Output
DSTBP3#	Y11	Source Sync	Input/Output
FERR#	E27	Async GTL+	Output
GTLREF	W23	Power/Other	Input
GTLREF	W9	Power/Other	Input
GTLREF	F23	Power/Other	Input
GTLREF	F9	Power/Other	Input
HIT#	E22	Common Clk	Input/Output
HITM#	A23	Common Clk	Input/Output
IERR#	E5	Async GTL+	Output

Table 34. Pin Listing by Pin Name

Pin Name	Pin No.	Signal Buffer Type	Direction
IGNNE#	C26	Async GTL+	Input
INIT#	D6	Async GTL+	Input
LINT0	B24	Async GTL+	Input
LINT1	G23	Async GTL+	Input
LOCK#	A17	Common Clk	Input/Output
MCERR#	D7	Common Clk	Input/Output
Mechanical Key	AE30		
ODTEN	B5	Power/Other	Input
PROCHOT#[3]	B25	Async GTL+	Input/Output
PWRGOOD	AB7	Async GTL+	Input
REQ0#	B19	Source Sync	Input/Output
REQ1#	B21	Source Sync	Input/Output
REQ2#	C21	Source Sync	Input/Output
REQ3#	C20	Source Sync	Input/Output
REQ4#	B22	Source Sync	Input/Output
Reserved	A1	Reserved	Reserved
Reserved	A4	Reserved	Reserved
Reserved	A15	Reserved	Reserved
Reserved	A16	Reserved	Reserved
Reserved	A26	Reserved	Reserved
Reserved	B1	Reserved	Reserved
Reserved	C5	Reserved	Reserved
Reserved	D25	Reserved	Reserved
Reserved	W3	Reserved	Reserved
Reserved	Y3	Reserved	Reserved
Reserved	Y29	Reserved	Reserved
Reserved	AA28	Reserved	Reserved
Reserved	AA29	Reserved	Reserved
Reserved	AB28	Reserved	Reserved
Reserved	AB29	Reserved	Reserved
Reserved	AC1	Reserved	Reserved
Reserved	AC28	Reserved	Reserved
Reserved	AC29	Reserved	Reserved
Reserved	AD1	Reserved	Reserved
Reserved	AD28	Reserved	Reserved

Table 34. Pin Listing by Pin Name

Pin Name	Pin No.	Signal Buffer Type	Direction
Reserved	AD29	Reserved	Reserved
Reserved	AE15	Reserved	Reserved
Reserved	AE16	Reserved	Reserved
RESET#	Y8	Common Clk	Input
RS0#	E21	Common Clk	Input
RS1#	D22	Common Clk	Input
RS2#	F21	Common Clk	Input
RSP#	C6	Common Clk	Input
SKTOCC#	A3	Power/Other	Output
SLP#	AE6	Async GTL+	Input
SMI#	C27	Async GTL+	Input
STPCLK#	D4	Async GTL+	Input
TCK	E24	TAP	Input
TDI	C24	TAP	Input
TDO	E25	TAP	Output
TESTHI0	W6	Power/Other	Input
TESTHI1	W7	Power/Other	Input
TESTHI2	W8	Power/Other	Input
TESTHI3	Y6	Power/Other	Input
TESTHI4	AA7	Power/Other	Input
TESTHI5	AD5	Power/Other	Input
TESTHI6	AE5	Power/Other	Input
THERMDA	Y27	Anode Pin	Output
THERMDC	Y28	Cathode Pin	Output
THERMTRIP#	F26	Async GTL+	Output
TMS	A25	TAP	Input
TRDY#	E19	Common Clk	Input
TRST#	F24	TAP	Input
VCC	A2	Power/Other	
VCC	A8	Power/Other	
VCC	A14	Power/Other	
VCC	A18	Power/Other	
VCC	A24	Power/Other	

Table 34. Pin Listing by Pin Name

Pin Name	Pin No.	Signal Buffer Type	Direction
VCC	A28	Power/Other	
VCC	A30	Power/Other	
VCC	B4	Power/Other	
VCC	B6	Power/Other	
VCC	B12	Power/Other	
VCC	B20	Power/Other	
VCC	B26	Power/Other	
VCC	B29	Power/Other	
VCC	B31	Power/Other	
VCC	C2	Power/Other	
VCC	C4	Power/Other	
VCC	C10	Power/Other	
VCC	C16	Power/Other	
VCC	C22	Power/Other	
VCC	C28	Power/Other	
VCC	C30	Power/Other	
VCC	D1	Power/Other	
VCC	D8	Power/Other	
VCC	D14	Power/Other	
VCC	D18	Power/Other	
VCC	D24	Power/Other	
VCC	D29	Power/Other	
VCC	D31	Power/Other	
VCC	E2	Power/Other	
VCC	E6	Power/Other	
VCC	E12	Power/Other	
VCC	E20	Power/Other	
VCC	E26	Power/Other	
VCC	E28	Power/Other	
VCC	E30	Power/Other	
VCC	F1	Power/Other	
VCC	F4	Power/Other	
VCC	F10	Power/Other	
VCC	F16	Power/Other	
VCC	F22	Power/Other	
VCC	F29	Power/Other	
VCC	F31	Power/Other	

Table 34. Pin Listing by Pin Name

Pin Name	Pin No.	Signal Buffer Type	Direction
VCC	G2	Power/Other	
VCC	G4	Power/Other	
VCC	G6	Power/Other	
VCC	G8	Power/Other	
VCC	G24	Power/Other	
VCC	G26	Power/Other	
VCC	G28	Power/Other	
VCC	G30	Power/Other	
VCC	H1	Power/Other	
VCC	H3	Power/Other	
VCC	H5	Power/Other	
VCC	H7	Power/Other	
VCC	H9	Power/Other	
VCC	H23	Power/Other	
VCC	H25	Power/Other	
VCC	H27	Power/Other	
VCC	H29	Power/Other	
VCC	H31	Power/Other	
VCC	J2	Power/Other	
VCC	J4	Power/Other	
VCC	J6	Power/Other	
VCC	J8	Power/Other	
VCC	J24	Power/Other	
VCC	J26	Power/Other	
VCC	J28	Power/Other	
VCC	J30	Power/Other	
VCC	K1	Power/Other	
VCC	K3	Power/Other	
VCC	K5	Power/Other	
VCC	K7	Power/Other	
VCC	K9	Power/Other	
VCC	K23	Power/Other	
VCC	K25	Power/Other	
VCC	K27	Power/Other	
VCC	K29	Power/Other	
VCC	K31	Power/Other	
VCC	L2	Power/Other	

Table 34. Pin Listing by Pin Name

Pin Name	Pin No.	Signal Buffer Type	Direction
VCC	L4	Power/Other	
VCC	L6	Power/Other	
VCC	L8	Power/Other	
VCC	L24	Power/Other	
VCC	L26	Power/Other	
VCC	L28	Power/Other	
VCC	L30	Power/Other	
VCC	M1	Power/Other	
VCC	M3	Power/Other	
VCC	M5	Power/Other	
VCC	M7	Power/Other	
VCC	M9	Power/Other	
VCC	M23	Power/Other	
VCC	M25	Power/Other	
VCC	M27	Power/Other	
VCC	M29	Power/Other	
VCC	M31	Power/Other	
VCC	N1	Power/Other	
VCC	N3	Power/Other	
VCC	N5	Power/Other	
VCC	N7	Power/Other	
VCC	N9	Power/Other	
VCC	N23	Power/Other	
VCC	N25	Power/Other	
VCC	N27	Power/Other	
VCC	N29	Power/Other	
VCC	N31	Power/Other	
VCC	P2	Power/Other	
VCC	P4	Power/Other	
VCC	P6	Power/Other	
VCC	P8	Power/Other	
VCC	P24	Power/Other	
VCC	P26	Power/Other	
VCC	P28	Power/Other	
VCC	P30	Power/Other	
VCC	R1	Power/Other	
VCC	R3	Power/Other	

Table 34. Pin Listing by Pin Name

Pin Name	Pin No.	Signal Buffer Type	Direction
VCC	R5	Power/Other	
VCC	R7	Power/Other	
VCC	R9	Power/Other	
VCC	R23	Power/Other	
VCC	R25	Power/Other	
VCC	R27	Power/Other	
VCC	R29	Power/Other	
VCC	R31	Power/Other	
VCC	T2	Power/Other	
VCC	T4	Power/Other	
VCC	T6	Power/Other	
VCC	T8	Power/Other	
VCC	T24	Power/Other	
VCC	T26	Power/Other	
VCC	T28	Power/Other	
VCC	T30	Power/Other	
VCC	U1	Power/Other	
VCC	U3	Power/Other	
VCC	U5	Power/Other	
VCC	U7	Power/Other	
VCC	U9	Power/Other	
VCC	U23	Power/Other	
VCC	U25	Power/Other	
VCC	U27	Power/Other	
VCC	U29	Power/Other	
VCC	U31	Power/Other	
VCC	V2	Power/Other	
VCC	V4	Power/Other	
VCC	V6	Power/Other	
VCC	V8	Power/Other	
VCC	V24	Power/Other	
VCC	V26	Power/Other	
VCC	V28	Power/Other	
VCC	V30	Power/Other	
VCC	W1	Power/Other	
VCC	W25	Power/Other	
VCC	W27	Power/Other	

Table 34. Pin Listing by Pin Name

Pin Name	Pin No.	Signal Buffer Type	Direction
VCC	W29	Power/Other	
VCC	W31	Power/Other	
VCC	Y10	Power/Other	
VCC	Y16	Power/Other	
VCC	Y2	Power/Other	
VCC	Y22	Power/Other	
VCC	Y30	Power/Other	
VCC	AA1	Power/Other	
VCC	AA4	Power/Other	
VCC	AA6	Power/Other	
VCC	AA12	Power/Other	
VCC	AA20	Power/Other	
VCC	AA26	Power/Other	
VCC	AA31	Power/Other	
VCC	AB2	Power/Other	
VCC	AB8	Power/Other	
VCC	AB14	Power/Other	
VCC	AB18	Power/Other	
VCC	AB24	Power/Other	
VCC	AB30	Power/Other	
VCC	AC3	Power/Other	
VCC	AC4	Power/Other	
VCC	AC10	Power/Other	
VCC	AC16	Power/Other	
VCC	AC22	Power/Other	
VCC	AC31	Power/Other	
VCC	AD2	Power/Other	
VCC	AD6	Power/Other	
VCC	AD12	Power/Other	
VCC	AD20	Power/Other	
VCC	AD26	Power/Other	
VCC	AD30	Power/Other	
VCC	AE3	Power/Other	
VCC	AE8	Power/Other	
VCC	AE14	Power/Other	
VCC	AE18	Power/Other	
VCC	AE24	Power/Other	

Table 34. Pin Listing by Pin Name

Pin Name	Pin No.	Signal Buffer Type	Direction
VCCA	AB4	Power/Other	Input
VCCIOPLL	AD4	Power/Other	Input
VCCSENSE	B27	Power/Other	Output
VID0	F3	Power/Other	Output
VID1	E3	Power/Other	Output
VID2	D3	Power/Other	Output
VID3	C3	Power/Other	Output
VID4	B3	Power/Other	Output
VID_V_{CC}	AE28	Power/Other	
VID_V_{CC}	AE29	Power/Other	
VSS	A5	Power/Other	
VSS	A11	Power/Other	
VSS	A21	Power/Other	
VSS	A27	Power/Other	
VSS	A29	Power/Other	
VSS	A31	Power/Other	
VSS	B2	Power/Other	
VSS	B9	Power/Other	
VSS	B15	Power/Other	
VSS	B17	Power/Other	
VSS	B23	Power/Other	
VSS	B28	Power/Other	
VSS	B30	Power/Other	
VSS	C1	Power/Other	
VSS	C7	Power/Other	
VSS	C13	Power/Other	
VSS	C19	Power/Other	
VSS	C25	Power/Other	
VSS	C29	Power/Other	
VSS	C31	Power/Other	
VSS	D2	Power/Other	
VSS	D5	Power/Other	
VSS	D11	Power/Other	
VSS	D21	Power/Other	
VSS	D27	Power/Other	
VSS	D28	Power/Other	
VSS	D30	Power/Other	

Table 34. Pin Listing by Pin Name

Pin Name	Pin No.	Signal Buffer Type	Direction
VSS	E1	Power/Other	
VSS	E9	Power/Other	
VSS	E15	Power/Other	
VSS	E17	Power/Other	
VSS	E23	Power/Other	
VSS	E29	Power/Other	
VSS	E31	Power/Other	
VSS	F2	Power/Other	
VSS	F7	Power/Other	
VSS	F13	Power/Other	
VSS	F19	Power/Other	
VSS	F25	Power/Other	
VSS	F28	Power/Other	
VSS	F30	Power/Other	
VSS	G1	Power/Other	
VSS	G3	Power/Other	
VSS	G5	Power/Other	
VSS	G7	Power/Other	
VSS	G9	Power/Other	
VSS	G25	Power/Other	
VSS	G27	Power/Other	
VSS	G29	Power/Other	
VSS	G31	Power/Other	
VSS	H2	Power/Other	
VSS	H4	Power/Other	
VSS	H6	Power/Other	
VSS	H8	Power/Other	
VSS	H24	Power/Other	
VSS	H26	Power/Other	
VSS	H28	Power/Other	
VSS	H30	Power/Other	
VSS	J1	Power/Other	
VSS	J3	Power/Other	
VSS	J5	Power/Other	
VSS	J7	Power/Other	
VSS	J9	Power/Other	
VSS	J23	Power/Other	

Table 34. Pin Listing by Pin Name

Pin Name	Pin No.	Signal Buffer Type	Direction
VSS	J25	Power/Other	
VSS	J27	Power/Other	
VSS	J29	Power/Other	
VSS	J31	Power/Other	
VSS	K2	Power/Other	
VSS	K4	Power/Other	
VSS	K6	Power/Other	
VSS	K8	Power/Other	
VSS	K24	Power/Other	
VSS	K26	Power/Other	
VSS	K28	Power/Other	
VSS	K30	Power/Other	
VSS	L1	Power/Other	
VSS	L3	Power/Other	
VSS	L5	Power/Other	
VSS	L7	Power/Other	
VSS	L9	Power/Other	
VSS	L23	Power/Other	
VSS	L25	Power/Other	
VSS	L27	Power/Other	
VSS	L29	Power/Other	
VSS	L31	Power/Other	
VSS	M2	Power/Other	
VSS	M4	Power/Other	
VSS	M6	Power/Other	
VSS	M8	Power/Other	
VSS	M24	Power/Other	
VSS	M26	Power/Other	
VSS	M28	Power/Other	
VSS	M30	Power/Other	
VSS	N2	Power/Other	
VSS	N4	Power/Other	
VSS	N6	Power/Other	
VSS	N8	Power/Other	
VSS	N24	Power/Other	
VSS	N26	Power/Other	
VSS	N28	Power/Other	

Table 34. Pin Listing by Pin Name

Pin Name	Pin No.	Signal Buffer Type	Direction
VSS	N30	Power/Other	
VSS	P1	Power/Other	
VSS	P3	Power/Other	
VSS	P5	Power/Other	
VSS	P7	Power/Other	
VSS	P9	Power/Other	
VSS	P23	Power/Other	
VSS	P25	Power/Other	
VSS	P27	Power/Other	
VSS	P29	Power/Other	
VSS	P31	Power/Other	
VSS	R2	Power/Other	
VSS	R4	Power/Other	
VSS	R6	Power/Other	
VSS	R8	Power/Other	
VSS	R24	Power/Other	
VSS	R26	Power/Other	
VSS	R28	Power/Other	
VSS	R30	Power/Other	
VSS	T1	Power/Other	
VSS	T3	Power/Other	
VSS	T5	Power/Other	
VSS	T7	Power/Other	
VSS	T9	Power/Other	
VSS	T23	Power/Other	
VSS	T25	Power/Other	
VSS	T27	Power/Other	
VSS	T29	Power/Other	
VSS	T31	Power/Other	
VSS	U2	Power/Other	
VSS	U4	Power/Other	
VSS	U6	Power/Other	
VSS	U8	Power/Other	
VSS	U24	Power/Other	
VSS	U26	Power/Other	
VSS	U28	Power/Other	
VSS	U30	Power/Other	

Table 34. Pin Listing by Pin Name

Pin Name	Pin No.	Signal Buffer Type	Direction
VSS	V1	Power/Other	
VSS	V3	Power/Other	
VSS	V5	Power/Other	
VSS	V7	Power/Other	
VSS	V9	Power/Other	
VSS	V23	Power/Other	
VSS	V25	Power/Other	
VSS	V27	Power/Other	
VSS	V29	Power/Other	
VSS	V31	Power/Other	
VSS	W2	Power/Other	
VSS	W4	Power/Other	
VSS	W24	Power/Other	
VSS	W26	Power/Other	
VSS	W28	Power/Other	
VSS	W30	Power/Other	
VSS	Y1	Power/Other	
VSS	Y5	Power/Other	
VSS	Y7	Power/Other	
VSS	Y13	Power/Other	
VSS	Y19	Power/Other	
VSS	Y25	Power/Other	
VSS	Y31	Power/Other	
VSS	AA2	Power/Other	
VSS	AA9	Power/Other	
VSS	AA15	Power/Other	
VSS	AA17	Power/Other	
VSS	AA23	Power/Other	
VSS	AA30	Power/Other	
VSS	AB1	Power/Other	
VSS	AB5	Power/Other	
VSS	AB11	Power/Other	
VSS	AB21	Power/Other	
VSS	AB27	Power/Other	
VSS	AB31	Power/Other	
VSS	AC2	Power/Other	
VSS	AC7	Power/Other	

Table 34. Pin Listing by Pin Name

Pin Name	Pin No.	Signal Buffer Type	Direction
VSS	AC13	Power/Other	
VSS	AC19	Power/Other	
VSS	AC25	Power/Other	
VSS	AC30	Power/Other	
VSS	AD3	Power/Other	
VSS	AD9	Power/Other	
VSS	AD15	Power/Other	
VSS	AD17	Power/Other	
VSS	AD23	Power/Other	
VSS	AD31	Power/Other	
VSS	AE2	Power/Other	
VSS	AE4	Power/Other	
VSS	AE11	Power/Other	
VSS	AE21	Power/Other	
VSS	AE27	Power/Other	
VSSA	AA5	Power/Other	Input
VSSSENSE	D26	Power/Other	Output

1. In systems utilizing the Low Voltage Xeon processor, the system designer must pull-up these signals to the processor V_{CC}.
2. Baseboard treating AA3 and AB3 as Reserved may operate correctly with a bus clock of 100 MHz.
3. It is an output only on 1.6 GHz Low Voltage Intel® Xeon™ processor with CPUID of 0F27h.

5.1.2 Pin Listing by Pin Number

Table 35. Pin Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type	Direction
A1	Reserved	Reserved	Reserved
A2	VCC	Power/Other	
A3	SKTOCC#	Power/Other	Output
A4	Reserved	Reserved	Reserved
A5	VSS	Power/Other	
A6	A32#	Source Sync	Input/Output
A7	A33#	Source Sync	Input/Output
A8	VCC	Power/Other	
A9	A26#	Source Sync	Input/Output
A10	A20#	Source Sync	Input/Output
A11	VSS	Power/Other	
A12	A14#	Source Sync	Input/Output
A13	A10#	Source Sync	Input/Output
A14	VCC	Power/Other	
A15	Reserved	Reserved	Reserved
A16	Reserved	Reserved	Reserved
A17	LOCK#	Common Clk	Input/Output
A18	VCC	Power/Other	
A19	A7#	Source Sync	Input/Output
A20	A4#	Source Sync	Input/Output
A21	VSS	Power/Other	
A22	A3#	Source Sync	Input/Output
A23	HITM#	Common Clk	Input/Output
A24	VCC	Power/Other	
A25	TMS	TAP	Input
A26	Reserved	Reserved	Reserved
A27	VSS	Power/Other	
A28	VCC	Power/Other	
A29	VSS	Power/Other	
A30	VCC	Power/Other	
A31	VSS	Power/Other	
B1	Reserved	Reserved	Reserved
B2	VSS	Power/Other	
B3	VID4	Power/Other	Output

Table 35. Pin Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type	Direction
B4	VCC	Power/Other	
B5	OTDEN	Power/Other	Input
B6	VCC	Power/Other	
B7	A31#	Source Sync	Input/Output
B8	A27#	Source Sync	Input/Output
B9	VSS	Power/Other	
B10	A21#	Source Sync	Input/Output
B11	A22#	Source Sync	Input/Output
B12	VCC	Power/Other	
B13	A13#	Source Sync	Input/Output
B14	A12#	Source Sync	Input/Output
B15	VSS	Power/Other	
B16	A11#	Source Sync	Input/Output
B17	VSS	Power/Other	
B18	A5#	Source Sync	Input/Output
B19	REQ0#	Common Clk	Input/Output
B20	VCC	Power/Other	
B21	REQ1#	Common Clk	Input/Output
B22	REQ4#	Common Clk	Input/Output
B23	VSS	Power/Other	
B24	LINT0	Async GTL+	Input
B25	PROCHOT#[3]	Power/Other	Input/Output
B26	VCC	Power/Other	
B27	VCCSENSE	Power/Other	Output
B28	VSS	Power/Other	
B29	VCC	Power/Other	
B30	VSS	Power/Other	
B31	VCC	Power/Other	
C1	VSS	Power/Other	
C2	VCC	Power/Other	
C3	VID3	Power/Other	Output
C4	VCC	Power/Other	
C5	Reserved	Reserved	Reserved
C6	RSP#	Common Clk	Input

Table 35. Pin Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type	Direction
C7	VSS	Power/Other	
C8	A35#	Source Sync	Input/Output
C9	A34#	Source Sync	Input/Output
C10	VCC	Power/Other	
C11	A30#	Source Sync	Input/Output
C12	A23#	Source Sync	Input/Output
C13	VSS	Power/Other	
C14	A16#	Source Sync	Input/Output
C15	A15#	Source Sync	Input/Output
C16	VCC	Power/Other	
C17	A8#	Source Sync	Input/Output
C18	A6#	Source Sync	Input/Output
C19	VSS	Power/Other	
C20	REQ3#	Common Clk	Input/Output
C21	REQ2#	Common Clk	Input/Output
C22	VCC	Power/Other	
C23	DEFER#	Common Clk	Input
C24	TDI	TAP	Input
C25	VSS	Power/Other	Input
C26	IGNNE#	Async GTL+	Input
C27	SMI#	Async GTL+	Input
C28	VCC	Power/Other	
C29	VSS	Power/Other	
C30	VCC	Power/Other	
C31	VSS	Power/Other	
D1	VCC	Power/Other	
D2	VSS	Power/Other	
D3	VID2	Power/Other	Output
D4	STPCLK#	Async GTL+	Input
D5	VSS	Power/Other	
D6	INIT#	Async GTL+	Input
D7	MCERR#	Common Clk	Input/Output
D8	VCC	Power/Other	
D9	AP1#	Common Clk	Input/Output

Table 35. Pin Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type	Direction
D10	BR3#[1]	Common Clk	Input
D11	VSS	Power/Other	
D12	A29#	Source Sync	Input/Output
D13	A25#	Source Sync	Input/Output
D14	VCC	Power/Other	
D15	A18#	Source Sync	Input/Output
D16	A17#	Source Sync	Input/Output
D17	A9#	Source Sync	Input/Output
D18	VCC	Power/Other	
D19	ADS#	Common Clk	Input/Output
D20	BR0#	Common Clk	Input/Output
D21	VSS	Power/Other	
D22	RS1#	Common Clk	Input
D23	BPRI#	Common Clk	Input
D24	VCC	Power/Other	
D25	Reserved	Reserved	Reserved
D26	VSSSENSE	Power/Other	Output
D27	VSS	Power/Other	
D28	VSS	Power/Other	
D29	VCC	Power/Other	
D30	VSS	Power/Other	
D31	VCC	Power/Other	
E1	VSS	Power/Other	
E2	VCC	Power/Other	
E3	VID1	Power/Other	Output
E4	BPM5#	Common Clk	Input/Output
E5	IERR#	Common Clk	Output
E6	VCC	Power/Other	
E7	BPM2#	Common Clk	Input/Output
E8	BPM4#	Common Clk	Input/Output
E9	VSS	Power/Other	
E10	AP0#	Common Clk	Input/Output

Table 35. Pin Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type	Direction
E11	BR2#[1]	Common Clk	Input
E12	VCC	Power/Other	
E13	A28#	Source Sync	Input/Output
E14	A24#	Source Sync	Input/Output
E15	VSS	Power/Other	
E16	COMP1	Power/Other	Input
E17	VSS	Power/Other	
E18	DRDY#	Common Clk	Input/Output
E19	TRDY#	Common Clk	Input
E20	VCC	Power/Other	
E21	RS0#	Common Clk	Input
E22	HIT#	Common Clk	Input/Output
E23	VSS	Power/Other	
E24	TCK	TAP	Input
E25	TDO	TAP	Output
E26	VCC	Power/Other	
E27	FERR#	Async GTL+	Output
E28	VCC	Power/Other	
E29	VSS	Power/Other	
E30	VCC	Power/Other	
E31	VSS	Power/Other	
F1	VCC	Power/Other	
F2	VSS	Power/Other	
F3	VID0	Power/Other	Output
F4	VCC	Power/Other	
F5	BPM3#	Common Clk	Input/Output
F6	BPM0#	Common Clk	Input/Output
F7	VSS	Power/Other	
F8	BPM1#	Common Clk	Input/Output
F9	GTLREF	Power/Other	Input
F10	VCC	Power/Other	
F11	BINIT#	Common Clk	Input/Output

Table 35. Pin Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type	Direction
F12	BR1#	Common Clk	Input
F13	VSS	Power/Other	
F14	ADSTB1#	Source Sync	Input/Output
F15	A19#	Source Sync	Input/Output
F16	VCC	Power/Other	
F17	ADSTB0#	Source Sync	Input/Output
F18	DBSY#	Common Clk	Input/Output
F19	VSS	Power/Other	
F20	BNR#	Common Clk	Input/Output
F21	RS2#	Common Clk	Input
F22	VCC	Power/Other	
F23	GTLREF	Power/Other	Input
F24	TRST#	TAP	Input
F25	VSS	Power/Other	
F26	THERMTRIP#	Async GTL+	Output
F27	A20M#	Async GTL+	Input
F28	VSS	Power/Other	
F29	VCC	Power/Other	
F30	VSS	Power/Other	
F31	VCC	Power/Other	
G1	VSS	Power/Other	
G2	VCC	Power/Other	
G3	VSS	Power/Other	
G4	VCC	Power/Other	
G5	VSS	Power/Other	
G6	VCC	Power/Other	
G7	VSS	Power/Other	
G8	VCC	Power/Other	
G9	VSS	Power/Other	
G23	LINT1	Async GTL+	Input
G24	VCC	Power/Other	
G25	VSS	Power/Other	
G26	VCC	Power/Other	
G27	VSS	Power/Other	
G28	VCC	Power/Other	

Table 35. Pin Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type	Direction
G29	VSS	Power/Other	
G30	VCC	Power/Other	
G31	VSS	Power/Other	
H1	VCC	Power/Other	
H2	VSS	Power/Other	
H3	VCC	Power/Other	
H4	VSS	Power/Other	
H5	VCC	Power/Other	
H6	VSS	Power/Other	
H7	VCC	Power/Other	
H8	VSS	Power/Other	
H9	VCC	Power/Other	
H23	VCC	Power/Other	
H24	VSS	Power/Other	
H25	VCC	Power/Other	
H26	VSS	Power/Other	
H27	VCC	Power/Other	
H28	VSS	Power/Other	
H29	VCC	Power/Other	
H30	VSS	Power/Other	
H31	VCC	Power/Other	
J1	VSS	Power/Other	
J2	VCC	Power/Other	
J3	VSS	Power/Other	
J4	VCC	Power/Other	
J5	VSS	Power/Other	
J6	VCC	Power/Other	
J7	VSS	Power/Other	
J8	VCC	Power/Other	
J9	VSS	Power/Other	
J23	VSS	Power/Other	
J24	VCC	Power/Other	
J25	VSS	Power/Other	
J26	VCC	Power/Other	
J27	VSS	Power/Other	
J28	VCC	Power/Other	
J29	VSS	Power/Other	
J30	VCC	Power/Other	

Table 35. Pin Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type	Direction
J31	VSS	Power/Other	
K1	VCC	Power/Other	
K2	VSS	Power/Other	
K3	VCC	Power/Other	
K4	VSS	Power/Other	
K5	VCC	Power/Other	
K6	VSS	Power/Other	
K7	VCC	Power/Other	
K8	VSS	Power/Other	
K9	VCC	Power/Other	
K23	VCC	Power/Other	
K24	VSS	Power/Other	
K25	VCC	Power/Other	
K26	VSS	Power/Other	
K27	VCC	Power/Other	
K28	VSS	Power/Other	
K29	VCC	Power/Other	
K30	VSS	Power/Other	
K31	VCC	Power/Other	
L1	VSS	Power/Other	
L2	VCC	Power/Other	
L3	VSS	Power/Other	
L4	VCC	Power/Other	
L5	VSS	Power/Other	
L6	VCC	Power/Other	
L7	VSS	Power/Other	
L8	VCC	Power/Other	
L9	VSS	Power/Other	
L23	VSS	Power/Other	
L24	VCC	Power/Other	
L25	VSS	Power/Other	
L26	VCC	Power/Other	
L27	VSS	Power/Other	
L28	VCC	Power/Other	
L29	VSS	Power/Other	
L30	VCC	Power/Other	
L31	VSS	Power/Other	
M1	VCC	Power/Other	

Table 35. Pin Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type	Direction
M2	VSS	Power/Other	
M3	VCC	Power/Other	
M4	VSS	Power/Other	
M5	VCC	Power/Other	
M6	VSS	Power/Other	
M7	VCC	Power/Other	
M8	VSS	Power/Other	
M9	VCC	Power/Other	
M23	VCC	Power/Other	
M24	VSS	Power/Other	
M25	VCC	Power/Other	
M26	VSS	Power/Other	
M27	VCC	Power/Other	
M28	VSS	Power/Other	
M29	VCC	Power/Other	
M30	VSS	Power/Other	
M31	VCC	Power/Other	
N1	VCC	Power/Other	
N2	VSS	Power/Other	
N3	VCC	Power/Other	
N4	VSS	Power/Other	
N5	VCC	Power/Other	
N6	VSS	Power/Other	
N7	VCC	Power/Other	
N8	VSS	Power/Other	
N9	VCC	Power/Other	
N23	VCC	Power/Other	
N24	VSS	Power/Other	
N25	VCC	Power/Other	
N26	VSS	Power/Other	
N27	VCC	Power/Other	
N28	VSS	Power/Other	
N29	VCC	Power/Other	
N30	VSS	Power/Other	
N31	VCC	Power/Other	
P1	VSS	Power/Other	
P2	VCC	Power/Other	
P3	VSS	Power/Other	

Table 35. Pin Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type	Direction
P4	VCC	Power/Other	
P5	VSS	Power/Other	
P6	VCC	Power/Other	
P7	VSS	Power/Other	
P8	VCC	Power/Other	
P9	VSS	Power/Other	
P23	VSS	Power/Other	
P24	VCC	Power/Other	
P25	VSS	Power/Other	
P26	VCC	Power/Other	
P27	VSS	Power/Other	
P28	VCC	Power/Other	
P29	VSS	Power/Other	
P30	VCC	Power/Other	
P31	VSS	Power/Other	
R1	VCC	Power/Other	
R2	VSS	Power/Other	
R3	VCC	Power/Other	
R4	VSS	Power/Other	
R5	VCC	Power/Other	
R6	VSS	Power/Other	
R7	VCC	Power/Other	
R8	VSS	Power/Other	
R9	VCC	Power/Other	
R23	VCC	Power/Other	
R24	VSS	Power/Other	
R25	VCC	Power/Other	
R26	VSS	Power/Other	
R27	VCC	Power/Other	
R28	VSS	Power/Other	
R29	VCC	Power/Other	
R30	VSS	Power/Other	
R31	VCC	Power/Other	
T1	VSS	Power/Other	
T2	VCC	Power/Other	
T3	VSS	Power/Other	
T4	VCC	Power/Other	
T5	VSS	Power/Other	

Table 35. Pin Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type	Direction
T6	VCC	Power/Other	
T7	VSS	Power/Other	
T8	VCC	Power/Other	
T9	VSS	Power/Other	
T23	VSS	Power/Other	
T24	VCC	Power/Other	
T25	VSS	Power/Other	
T26	VCC	Power/Other	
T27	VSS	Power/Other	
T28	VCC	Power/Other	
T29	VSS	Power/Other	
T30	VCC	Power/Other	
T31	VSS	Power/Other	
U1	VCC	Power/Other	
U2	VSS	Power/Other	
U3	VCC	Power/Other	
U4	VSS	Power/Other	
U5	VCC	Power/Other	
U6	VSS	Power/Other	
U7	VCC	Power/Other	
U8	VSS	Power/Other	
U9	VCC	Power/Other	
U23	VCC	Power/Other	
U24	VSS	Power/Other	
U25	VCC	Power/Other	
U26	VSS	Power/Other	
U27	VCC	Power/Other	
U28	VSS	Power/Other	
U29	VCC	Power/Other	
U30	VSS	Power/Other	
U31	VCC	Power/Other	
V1	VSS	Power/Other	
V2	VCC	Power/Other	
V3	VSS	Power/Other	
V4	VCC	Power/Other	
V5	VSS	Power/Other	
V6	VCC	Power/Other	
V7	VSS	Power/Other	

Table 35. Pin Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type	Direction
V8	VCC	Power/Other	
V9	VSS	Power/Other	
V23	VSS	Power/Other	
V24	VCC	Power/Other	
V25	VSS	Power/Other	
V26	VCC	Power/Other	
V27	VSS	Power/Other	
V28	VCC	Power/Other	
V29	VSS	Power/Other	
V30	VCC	Power/Other	
V31	VSS	Power/Other	
W1	VCC	Power/Other	
W2	VSS	Power/Other	
W3	Reserved	Reserved	Reserved
W4	VSS	Power/Other	
W5	BCLK1	Sys Bus Clk	Input
W6	TESTHI0	Power/Other	Input
W7	TESTHI1	Power/Other	Input
W8	TESTHI2	Power/Other	Input
W9	GTLREF	Power/Other	Input
W23	GTLREF	Power/Other	Input
W24	VSS	Power/Other	
W25	VCC	Power/Other	
W26	VSS	Power/Other	
W27	VCC	Power/Other	
W28	VSS	Power/Other	
W29	VCC	Power/Other	
W30	VSS	Power/Other	
W31	VCC	Power/Other	
Y1	VSS	Power/Other	
Y2	VCC	Power/Other	
Y3	Reserved	Reserved	Reserved
Y4	BCLK0	Sys Bus Clk	Input
Y5	VSS	Power/Other	
Y6	TESTHI3	Power/Other	Input
Y7	VSS	Power/Other	
Y8	RESET#	Common Clk	Input

Table 35. Pin Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type	Direction
Y9	D62#	Source Sync	Input/Output
Y10	VCC	Power/Other	
Y11	DSTBP3#	Source Sync	Input/Output
Y12	DSTBN3#	Source Sync	Input/Output
Y13	VSS	Power/Other	
Y14	DSTBP2#	Source Sync	Input/Output
Y15	DSTBN2#	Source Sync	Input/Output
Y16	VCC	Power/Other	
Y17	DSTBP1#	Source Sync	Input/Output
Y18	DSTBN1#	Source Sync	Input/Output
Y19	VSS	Power/Other	
Y20	DSTBP0#	Source Sync	Input/Output
Y21	DSTBN0#	Source Sync	Input/Output
Y22	VCC	Power/Other	
Y23	D5#	Source Sync	Input/Output
Y24	D2#	Source Sync	Input/Output
Y25	VSS	Power/Other	
Y26	D0#	Source Sync	Input/Output
Y27	THERMDA	Anode Pin	Output
Y28	THERMDC	Cathode Pin	Output
Y29	Reserved	Reserved	Reserved
Y30	VCC	Power/Other	
Y31	VSS	Power/Other	
AA1	VCC	Power/Other	
AA2	VSS	Power/Other	
AA3	BSEL0[2]	Power/Other	Output
AA4	VCC	Power/Other	
AA5	VSSA	Power/Other	Input
AA6	VCC	Power/Other	
AA7	TESTHI4	Power/Other	Input
AA8	D61#	Source Sync	Input/Output
AA9	VSS	Power/Other	
AA10	D54#	Source Sync	Input/Output
AA11	D53#	Source Sync	Input/Output
AA12	VCC	Power/Other	
AA13	D48#	Source Sync	Input/Output
AA14	D49#	Source Sync	Input/Output
AA15	VSS	Power/Other	

Table 35. Pin Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type	Direction
AA16	D33#	Source Sync	Input/Output
AA17	VSS	Power/Other	
AA18	D24#	Source Sync	Input/Output
AA19	D15#	Source Sync	Input/Output
AA20	VCC	Power/Other	
AA21	D11#	Source Sync	Input/Output
AA22	D10#	Source Sync	Input/Output
AA23	VSS	Power/Other	
AA24	D6#	Source Sync	Input/Output
AA25	D3#	Source Sync	Input/Output
AA26	VCC	Power/Other	
AA27	D1#	Source Sync	Input/Output
AA28	Reserved	Reserved	Reserved
AA29	Reserved	Reserved	Reserved
AA30	VSS	Power/Other	
AA31	VCC	Power/Other	
AB1	VSS	Power/Other	
AB2	VCC	Power/Other	
AB3	BSEL1[2]	Power/Other	Output
AB4	VCCA	Power/Other	Input
AB5	VSS	Power/Other	
AB6	D63#	Source Sync	
AB7	PWRGOOD	Power/Other	Input
AB8	VCC	Power/Other	
AB9	DBI3#	Source Sync	Input/Output
AB10	D55#	Source Sync	Input/Output
AB11	VSS	Power/Other	
AB12	D51#	Source Sync	Input/Output
AB13	D52#	Source Sync	Input/Output
AB14	VCC	Power/Other	
AB15	D37#	Source Sync	Input/Output
AB16	D32#	Source Sync	Input/Output
AB17	D31#	Source Sync	Input/Output
AB18	VCC	Power/Other	
AB19	D14#	Source Sync	Input/Output
AB20	D12#	Source Sync	Input/Output
AB21	VSS	Power/Other	
AB22	D13#	Source Sync	Input/Output

Table 35. Pin Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type	Direction
AB23	D9#	Source Sync	Input/Output
AB24	VCC	Power/Other	
AB25	D8#	Source Sync	Input/Output
AB26	D7#	Source Sync	Input/Output
AB27	VSS	Power/Other	
AB28	Reserved	Reserved	Reserved
AB29	Reserved	Reserved	Reserved
AB30	VCC	Power/Other	
AB31	VSS	Power/Other	
AC1	Reserved	Reserved	Reserved
AC2	VSS	Power/Other	
AC3	VCC	Power/Other	
AC4	VCC	Power/Other	
AC5	D60#	Source Sync	Input/Output
AC6	D59#	Source Sync	Input/Output
AC7	VSS	Power/Other	
AC8	D56#	Source Sync	Input/Output
AC9	D47#	Source Sync	Input/Output
AC10	VCC	Power/Other	
AC11	D43#	Source Sync	Input/Output
AC12	D41#	Source Sync	Input/Output
AC13	VSS	Power/Other	
AC14	D50#	Source Sync	Input/Output
AC15	DP2#	Common Clk	Input/Output
AC16	VCC	Power/Other	
AC17	D34#	Source Sync	Input/Output
AC18	DP0#	Common Clk	Input/Output
AC19	VSS	Power/Other	
AC20	D25#	Source Sync	Input/Output
AC21	D26#	Source Sync	Input/Output
AC22	VCC	Power/Other	
AC23	D23#	Source Sync	Input/Output
AC24	D20#	Source Sync	Input/Output
AC25	VSS	Power/Other	
AC26	D17#	Source Sync	Input/Output
AC27	DBI0#	Source Sync	Input/Output

Table 35. Pin Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type	Direction
AC28	Reserved	Reserved	Reserved
AC29	Reserved	Reserved	Reserved
AC30	VSS	Power/Other	
AC31	VCC	Power/Other	
AD1	Reserved	Reserved	Reserved
AD2	VCC	Power/Other	
AD3	VSS	Power/Other	
AD4	VCCIOPLL	Power/Other	Input
AD5	TESTHI5	Power/Other	Input
AD6	VCC	Power/Other	
AD7	D57#	Source Sync	Input/Output
AD8	D46#	Source Sync	Input/Output
AD9	VSS	Power/Other	
AD10	D45#	Source Sync	Input/Output
AD11	D40#	Source Sync	Input/Output
AD12	VCC	Power/Other	
AD13	D38#	Source Sync	Input/Output
AD14	D39#	Source Sync	Input/Output
AD15	VSS	Power/Other	
AD16	COMP0	Power/Other	Input
AD17	VSS	Power/Other	
AD18	D36#	Source Sync	Input/Output
AD19	D30#	Source Sync	Input/Output
AD20	VCC	Power/Other	
AD21	D29#	Source Sync	Input/Output
AD22	DBI1#	Source Sync	Input/Output
AD23	VSS	Power/Other	
AD24	D21#	Source Sync	Input/Output
AD25	D18#	Source Sync	Input/Output
AD26	VCC	Power/Other	
AD27	D4#	Source Sync	Input/Output
AD28	Reserved	Reserved	Reserved
AD29	Reserved	Reserved	Reserved
AD30	VCC	Power/Other	
AD31	VSS	Power/Other	
AE2	VSS	Power/Other	
AE3	VCC	Power/Other	
AE4	VSS	Power/Other	

Table 35. Pin Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type	Direction
AE5	TESTHI6	Power/Other	Input
AE6	SLP#	Async GTL+	Input
AE7	D58#	Source Sync	Input/Output
AE8	VCC	Power/Other	
AE9	D44#	Source Sync	Input/Output
AE10	D42#	Source Sync	Input/Output
AE11	VSS	Power/Other	
AE12	DBI2#	Source Sync	Input/Output
AE13	D35#	Source Sync	Input/Output
AE14	VCC	Power/Other	
AE15	Reserved	Reserved	Reserved
AE16	Reserved	Reserved	Reserved
AE17	DP3#	Common Clk	Input/Output
AE18	VCC	Power/Other	
AE19	DP1#	Common Clk	Input/Output
AE20	D28#	Source Sync	Input/Output
AE21	VSS	Power/Other	
AE22	D27#	Source Sync	Input/Output
AE23	D22#	Source Sync	Input/Output
AE24	VCC	Power/Other	
AE25	D19#	Source Sync	Input/Output
AE26	D16#	Source Sync	Input/Output
AE27	VSS	Power/Other	
AE28	VID_V_{CC}	Power/Other	
AE29	VID_V_{CC}	Power/Other	
AE30	Mechanical Key		

1. In systems utilizing the Low Voltage Xeon processor, the system designer must pull-up these signals to the processor V_{CC}.
2. Baseboards treating AA3 and AB3 as Reserved may operate correctly with a bus clock of 100 MHz.
3. It is an output only on 1.6 GHz Low Voltage Intel® Xeon™ processor with CPUID of 0F27h.

5.2 Signal Definitions

Table 36. Signal Definitions (Sheet 1 of 9)

Name	Type	Description
A[35:3]#	I/O	A[35:3]# (Address) define a 2^{36} byte physical memory address space. In sub-phase 1 of the address phase, these pins transmit the address of a transaction. In sub-phase 2, these pins transmit transaction type information. These signals must connect the appropriate pins of all agents on the system bus. A[35:3]# are protected by parity signals AP[1:0]#. A[35:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. On the active-to-inactive transition of RESET#, the processors sample a subset of the A[35:3]# pins to determine their power-on configuration. See Section 7.1.
A20M#	I	When A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1 MByte boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O write bus transaction.
ADS#	I/O	ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[35:3]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction. This signal must connect the appropriate pins on all system bus agents.
ADSTB[1:0]#	I/O	Address strobes are used to latch A[35:3]# and REQ[4:0]# on their rising and falling edge.
AP[1:0]#	I/O	AP[1:0]# (Address Parity) are driven by the request initiator along with ADS#, A[35:3]#, and the transaction type on the REQ[4:0]# pins. A correct parity signal is high when an even number of covered signals are low and low when an odd number of covered signals are low. This allows parity to be high when all the covered signals are high. AP[1:0]# should connect the appropriate pins of all system bus agents. The following table defines the coverage model of these signals.

Request Signals	Subphase 1	Subphase 2
A[35:24]#	AP0#	AP1#
A[23:3]#	AP1#	AP0#
REQ[4:0]#	AP1#	AP0#

BCLK[1:0]	I	The differential pair BCLK (Bus Clock) determines the bus frequency. All processor system bus agents must receive these signals to drive their outputs and latch their inputs. All external timing parameters are specified with respect to the rising edge of BCLK0 crossing the falling edge of BCLK1.

Table 36. Signal Definitions (Sheet 2 of 9)

Name	Type	Description
BINIT#	I/O	BINIT# (Bus Initialization) may be observed and driven by all processor system bus agents and when used, must connect the appropriate pins of all such agents. When the BINIT# driver is enabled during power on configuration, BINIT# is asserted to signal any bus condition that prevents reliable future information. When BINIT# observation is enabled during power-on configuration (see Section 7.1) and BINIT# is sampled asserted, symmetric agents reset their bus LOCK# activity and bus request arbitration state machines. The bus agents **do not** reset their IOQ and transaction tracking state machines upon observation of BINIT# assertion. Once the BINIT# assertion has been observed, the bus agents will re-arbitrate for the system bus and attempt completion of their bus queue and IOQ entries. When BINIT# observation is disabled during power-on configuration, a central agent may handle an assertion of BINIT# as appropriate to the error handling architecture of the system.
BNR#	I/O	BNR# (Block Next Request) is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions. Since multiple agents might need to request a bus stall at the same time, BNR# is a wire-OR signal which must connect the appropriate pins of all processor system bus agents. In order to avoid wire-OR glitches associated with simultaneous edge transitions driven by multiple drivers, BNR# is activated on specific clock edges and sampled on specific clock edges.
BPM[5:0]#	I/O	BPM[5:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[5:0]# should connect the appropriate pins of all system bus agents. BPM4# provides PRDY# (Probe Ready) functionality for the TAP port. PRDY# is a processor output used by debug tools to determine processor debug readiness. BPM5# provides PREQ# (Probe Request) functionality for the TAP port. PREQ# is used by debug tools to request debug operation of the processors. BPM[5:4]# must be bussed to all bus agents. **These signals do not have on-die termination and must be terminated at the end agent. See the appropriate platform design guidelines for additional information.**
BPRI#	I	BPRI# (Bus Priority Request) is used to arbitrate for ownership of the processor system bus. It must connect the appropriate pins of all processor system bus agents. Observing BPRI# active (as asserted by the priority agent) causes all other agents to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.

Table 36. Signal Definitions (Sheet 3 of 9)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>BR0#
BR[1:3]#</td><td>I/O
I</td><td>BR[3:0]# (Bus Request) drive the BREQ[3:0]# signals in the system. The BREQ[3:0]# signals are interconnected in a rotating manner to individual processor pins. BR2# and BR3# must not be utilized in a dual processor platform design. The table below gives the rotating interconnect between the processor and bus signals for dual processor systems.
BR[1:0]# Signals Rotating Interconnect, dual processor system
<table>
<tr><th>Bus Signal</th><th>Agent 0 Pins</th><th>Agent 1 Pins</th></tr>
<tr><td>BREQ0#</td><td>BR0#</td><td>BR1#</td></tr>
<tr><td>BREQ1#</td><td>BR1#</td><td>BR0#</td></tr>
</table>
During power-up configuration, the central agent must assert the BR0# bus signal. All symmetric agents sample their BR[1:0]# pins on active-to-inactive transition of RESET#. The pin on which the agent samples an active level determines its agent ID. All agents then configure their pins to match the appropriate bus signal protoco as shown below.
BR[1:0]# Signal Agent IDs
<table>
<tr><th>BR[1:0]# Signals Rotating Interconnect, dual processor system</th><th>Agent ID</th></tr>
<tr><td>BR0#</td><td>0</td></tr>
<tr><td>BR1#</td><td>1</td></tr>
</table>
During power-on configuration, the central agent must assert the BR0# bus signal. All symmetric agents sample their BR[3:0]# pins on the active-to-inactive transition of RESET#. The pin which the agent samples asserted determines it’s agent ID.
These signals do not have on-die termination and must be terminated at the end agent. See the appropriate platform design guidelines for additional information.</td></tr>
<tr><td>BSEL[1:0]</td><td>O</td><td>These output signals are used to select the system bus frequency.
A BSEL[1:0] = 00 will select a 100 MHz bus clock frequency. The frequency is determined by the processor(s), chipset, and frequency synthesizer capabilities. All system bus agents must operate at the same frequency. Individual processors will only operate at their specified front side bus (FSB) frequency.
On baseboards which support operation only at 100 MHz bus clocks these signals may be ignored. On baseboards employing the use of these signals, a 1 KΩ pull-up resistor be used.
See Table 3, “System Bus Clock Frequency Select Truth Table for BSEL[1:0]” on page 15 for output values.</td></tr>
<tr><td>COMP[1:0]</td><td>I</td><td>COMP[1:0] must be terminated to V_{SS} on the baseboard using precision resistors. These inputs configure the AGTL+ drivers of the processor. Refer to the appropriate platform design guidelines and Table 12 for implementation details.</td></tr>
</table>

Table 36. Signal Definitions (Sheet 4 of 9)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>D[63:0]#</td><td>I/O</td><td>D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the processor system bus agents, and must connect the appropriate pins on all such agents. The data driver asserts DRDY# to indicate a valid data transfer.
D[63:0]# are quad-pumped signals, and will thus be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to strobes and DBI#.

<table><tr><th>Data Group</th><th>DSTBN/ DSTBP</th><th>DBI#</th></tr><tr><td>D[15:0]#</td><td>0</td><td>0</td></tr><tr><td>D[31:16]#</td><td>1</td><td>1</td></tr><tr><td>D[47:32]#</td><td>2</td><td>2</td></tr><tr><td>D[63:48]#</td><td>3</td><td>3</td></tr></table>Furthermore, the DBI# pins determine the polarity of the data signals. Each group of 16 data signals corresponds to one DBI# signal. When the DBI# signal is active, the corresponding data group is inverted and therefore sampled active high.</td></tr>
<tr><td>DBI[3:0]#</td><td>I/O</td><td>DBI[3:0]# are source synchronous and indicate the polarity of the D[63:0]# signals. The DBI[3:0]# signals are activated when the data on the data bus is inverted. The bus agent will invert the data bus signals when more than half the bits, within a 16-bit group, change logic level in the next cycle.

DBI[3:0] Assignment To Data Bus
<table><tr><th>Bus Signal</th><th>Data Bus Signals</th></tr><tr><td>DBI0#</td><td>D[15:0]#</td></tr><tr><td>DBI1#</td><td>D[31:16]#</td></tr><tr><td>DBI2#</td><td>D[47:32]#</td></tr><tr><td>DBI3#</td><td>D[63:48]#</td></tr></table></td></tr>
<tr><td>DBSY#</td><td>I/O</td><td>DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the processor system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on all processor system bus agents.</td></tr>
<tr><td>DEFER#</td><td>I</td><td>DEFER# is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or I/O agent. This signal must connect the appropriate pins of all processor system bus agents.</td></tr>
<tr><td>DP[3:0]#</td><td>I/O</td><td>DP[3:0]# (Data Parity) provide parity protection for the D[63:0]# signals. They are driven by the agent responsible for driving D[63:0]#, and must connect the appropriate pins of all processor system bus agents.</td></tr>
<tr><td>DRDY#</td><td>I/O</td><td>DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of all processor system bus agents.</td></tr>
<tr><td>DSTBN[3:0]#</td><td>I/O</td><td>Data strobe used to latch in D[63:0]#.</td></tr>
<tr><td>DSTBP[3:0]#</td><td>I/O</td><td>Data strobe used to latch in D[63:0]#.</td></tr>
</table>

Table 36. Signal Definitions (Sheet 5 of 9)

Name	Type	Description
FERR#/PBE#	O	FERR#/PBE# (floating point error/pending break event) is a multiplexed signal and its meaning is qualified by STPCLK#. When STPCLK# is not asserted, FERR#/PBE# indicates a floating-point error and will be asserted when the processor detects an unmasked floating-point error. When STPCLK# is not asserted, FERR#/PBE# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MS-DOS*-type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR#/PBE# indicates that the processor has a pending break event waiting for service. The assertion of FERR#/PBE# indicates that the processor should be returned to the Normal state. For additional information on the pending break event functionality, including the identification of support of the feature and enable/disable information, refer to volume 3 of the Intel Architecture Software Developer's Manual and the Intel Processor Identification and the CPUID Instruction application note. **This signal does not have on-die termination and must be terminated at the end agent. See the appropriate Platform Design Guideline for additional information.**
GTLREF	I	GTLREF determines the signal reference level for AGTL+ input pins. GTLREF should be set at 0.63 Vcc. GTLREF is used by the AGTL+ receivers to determine when a signal is a logical 0 or a logical 1.
HIT# **HITM#**	I/O I/O	HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Any system bus agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which may be continued by reasserting HIT# and HITM# together. Since multiple agents may deliver snoop results at the same time, HIT# and HITM# are wire-OR signals which must connect the appropriate pins of all processor system bus agents. In order to avoid wire-OR glitches associated with simultaneous edge transitions driven by multiple drivers, HIT# and HITM# are activated on specific clock edges and sampled on specific clock edges.
IERR#	O	IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the processor system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#. **This signal does not have on-die termination and must be terminated at the end agent. See the appropriate Platform Design Guideline for additional information.**
IGNNE#	I	IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. When IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction when a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O write bus transaction.
INIT#	I	INIT# (Initialization), when asserted, resets integer registers inside all processors without affecting their internal caches or floating-point registers. Each processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal and must connect the appropriate pins of all processor system bus agents. When INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST).

Table 36. Signal Definitions (Sheet 6 of 9)

Name	Type	Description
LINT[1:0]	I	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all system bus agents. When the APIC functionality is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.
LOCK#	I/O	LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of all processor system bus agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the processor system bus, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the processor system bus throughout the bus locked operation and ensure the atomicity of lock.
MCERR#	I/O	MCERR# (Machine Check Error) is asserted to indicate an unrecoverable error without a bus protocol violation. It may be driven by all processor system bus agents. MCERR# assertion conditions are configurable at a system level. Assertion options are defined by the following options: • Enabled or disabled. • Asserted, when configured, for internal errors along with IERR#. • Asserted, when configured, by the request initiator of a bus transaction after it observes an error. • Asserted by any bus agent when it observes an error in a bus transaction. For more details regarding machine check architecture, refer to the *IA-32 Software Developer's Manual, Volume 3: System Programming Guide*. Since multiple agents may drive this signal at the same time, MCERR# is a wire-OR signal which must connect the appropriate pins of all processor system bus agents. In order to avoid wire-OR glitches associated with simultaneous edge transitions driven by multiple drivers, MCERR# is activated on specific clock edges and sampled on specific clock edges.
Mechanical Key	Inert	The mechanical key is to prevent compatibility with 603-pin socket.
ODTEN	I	ODTEN (On-die termination enable) should be connected to V_{CC} to enable on-die termination for end bus agents. For middle bus agents, pull this signal down via a resistor to ground to disable on-die termination. Whenever ODTEN is high, on-die termination will be active, regardless of other states of the bus.
PROCHOT#	I/O	PROCHOT# As an output, PROCHOT# (Processor Hot) will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. As an input, assertion of PROCHOT# by the system will activate the TCC, if enabled. The TCC will remain active until the system deasserts PROCHOT#. See Section 7.3 for more details. The PROCHOT# is an output only on 1.6 GHz Low Voltage Intel® Xeon™ processor with CPUID of 0F27h.

Table 36. Signal Definitions (Sheet 7 of 9)

Name	Type	Description
PWRGOOD	I	PWRGOOD (Power Good) is an input. The processor requires this signal to be a clean indication that all processor clocks and power supplies are stable and within their specifications. “Clean” implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. Figure 12 illustrates the relationship of PWRGOOD to the RESET# signal. PWRGOOD may be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. It must also meet the minimum pulse width specification in Table 14, and be followed by a 1 mS RESET# pulse. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.
REQ[4:0]#	I/O	REQ[4:0]# (Request Command) must connect the appropriate pins of all processor system bus agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB[1:0]#. Refer to the AP[1:0]# signal description for details on parity checking of these signals.
RESET#	I	Asserting the RESET# signal resets all processors to known states and invalidates their internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least one millisecond after VCC and BCLK have reached their proper specifications. On observing active RESET#, all system bus agents will deassert their outputs within two clocks. RESET# must not be kept asserted for more than 10ms. A number of bus signals are sampled at the active-to-inactive transition of RESET# for power-on configuration. These configuration options are described in the Section 7.1. **This signal does not have on-die termination and must be terminated at the end agent. See the appropriate Platform Design Guideline for additional information.**
RS[2:0]#	I	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of all processor system bus agents.
RSP#	I	RSP# (Response Parity) is driven by the response agent (the agent responsible for completion of the current transaction) during assertion of RS[2:0]#, the signals for which RSP# provides parity protection. It must connect to the appropriate pins of all processor system bus agents. A correct parity signal is high when an even number of covered signals are low and low when an odd number of covered signals are low. While RS[2:0]# = 000, RSP# is also high, since this indicates it is not being driven by any agent guaranteeing correct parity.
SKTOCC#	O	SKTOCC# (Socket occupied) will be pulled to ground by the processor to indicate that the processor is present.
SLP#	I	SLP# (Sleep), when asserted in Stop-Grant state, causes processors to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertion of the RESET# signal, deassertion of SLP#, and removal of the BCLK input while in Sleep state. When SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units.

Table 36. Signal Definitions (Sheet 8 of 9)

Name	Type	Description
SMI#	I	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, processors save the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. When SMI# is asserted during the deassertion of RESET# the processor will tri-state its outputs.
STPCLK#	I	STPCLK# (Stop Clock), when asserted, causes processors to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the system bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
TCK	I	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).
TDI	I	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	O	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TESTHI[6:0]	I	All TESTHI[6:0] pins should be individually connected to V_{CC} via a pull-up resistor which matches the trace impedance within a range of ±10 ohms. TESTHI[3:0] and TESTHI[6:5] may all be tied together and pulled up to V_{CC} with a single resistor when desired. However, utilization of boundary scan test will not be functional when these pins are connected together. TESTHI4 must always be pulled up independently from the other TESTHI pins. For optimum noise margin, all pull-up resistor values used for TESTHI[6:0] pins should have a resistance value within ±20 percent of the impedance of the baseboard transmission line traces. For example, when the trace impedance is 50 Ω, then a value between 40 Ω and 60 Ω should be used. The TESTHI[6:0] termination recommendations provided in the Intel® Xeon™ processor datasheet are still suitable for the Intel® Xeon™ processor with 512 KB L2 cache. However, Intel recommends new designs or designs undergoing design updates follow the trace impedance matching termination guidelines given in this section.
THERMDA	O	Thermal Diode Anode
THERMDC	O	Thermal Diode Cathode
THERMTRIP#	O	Activation of THERMTRIP# (Thermal Trip) indicates the processor junction temperature has reached a level beyond which permanent silicon damage may occur. Measurement of the temperature is accomplished through an internal thermal sensor which is configured to trip at approximately 135 °C. To properly protect the processor, power must be removed upon THERMTRIP# becoming active. See Figure 15, “THERMTRIP# to VCC Timing” on page 37 for the appropriate power down sequence and timing requirement. In parallel, the processor will attempt to reduce its temperature by shutting off internal clocks and stopping all program execution. Once activated, THERMTRIP# remains latched and the processor will be stopped until RESET# is asserted. A RESET# pulse will reset the processor and execution will begin at the boot vector. When the temperature has not dropped below the trip level, the processor will assert THERMTRIP# and return to the shutdown state. The processor releases THERMTRIP# when RESET# is activated even when the processor is still too hot. **This signal do not have on-die termination and must be terminated at the end agent. See the appropriate platform design guidelines for additional information**.

Table 36. Signal Definitions (Sheet 9 of 9)

Name	Type	Description
TMS	I	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools. **This signal does not have on-die termination and must be terminated at the end agent. See the appropriate platform design guidelines for additional information**.
TRDY#	I	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of all system bus agents.
TRST#	I	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset. **See the appropriate Platform Design Guideline for additional information**.
V_{CCA}	I	VCCA provides isolated power for the analog portion of the internal PLL's. Use a discrete RLC filter to provide clean power. Use the filter defined in Section 2.5 to provide clean power to the PLL. The tolerance and total ESR for the filter is important. Refer to the appropriate platform design guidelines for complete implementation details.
$V_{CCIOPLL}$	I	$V_{CCIOPLL}$ provides isolated power for digital portion of the internal PLL's. Follow the guidelines for V_{CCA} (Section 2.5), and refer to the appropriate platform design guidelines for complete implementation details.
$V_{CCSENSE}$ **$V_{SSSENSE}$**	O	The Vccsense and Vsssense pins are the points for which processor minimum and maximum voltage requirements are specified. Uniprocessor designs may utilize these pins for voltage sensing for the processor's voltage regulator. However, multiprocessor designs must not connect these pins to sense logic, but rather utilize them for power delivery validation.
VID[4:0]	O	VID[4:0] (Voltage ID) pins may be used to support automatic selection of power supply voltages (V_{CC}). Unlike previous processor generations, these pins are driven by processor logic. Hence the voltage supply for these pins (VID_V_{CC}) must be valid before the VRM supplying Vcc to the processor is enabled. Conversely, the VRM output must be disabled prior to the voltage supply for these pins becomes invalid. The VID pins are needed to support processor voltage specification variations. See Table 4 for definitions of these pins. The power supply must supply the voltage that is requested by these pins, or disable itself.
VID_V_{CC}	I	Voltage for VID and BSEL logic.
V_{SSA}	I	V_{SSA} provides an isolated, **internal** ground for internal PLL's. Do not connect directly to ground. This pin is to be connected to V_{CCA} and $V_{CCIOPLL}$ through a discrete filter circuit.

Note: Low Voltage Intel Xeon processors only support BR0# and BR1#. However, the Low Voltage Intel Xeon processors must terminate BR2# and BR3# to the processor V_{CC}.

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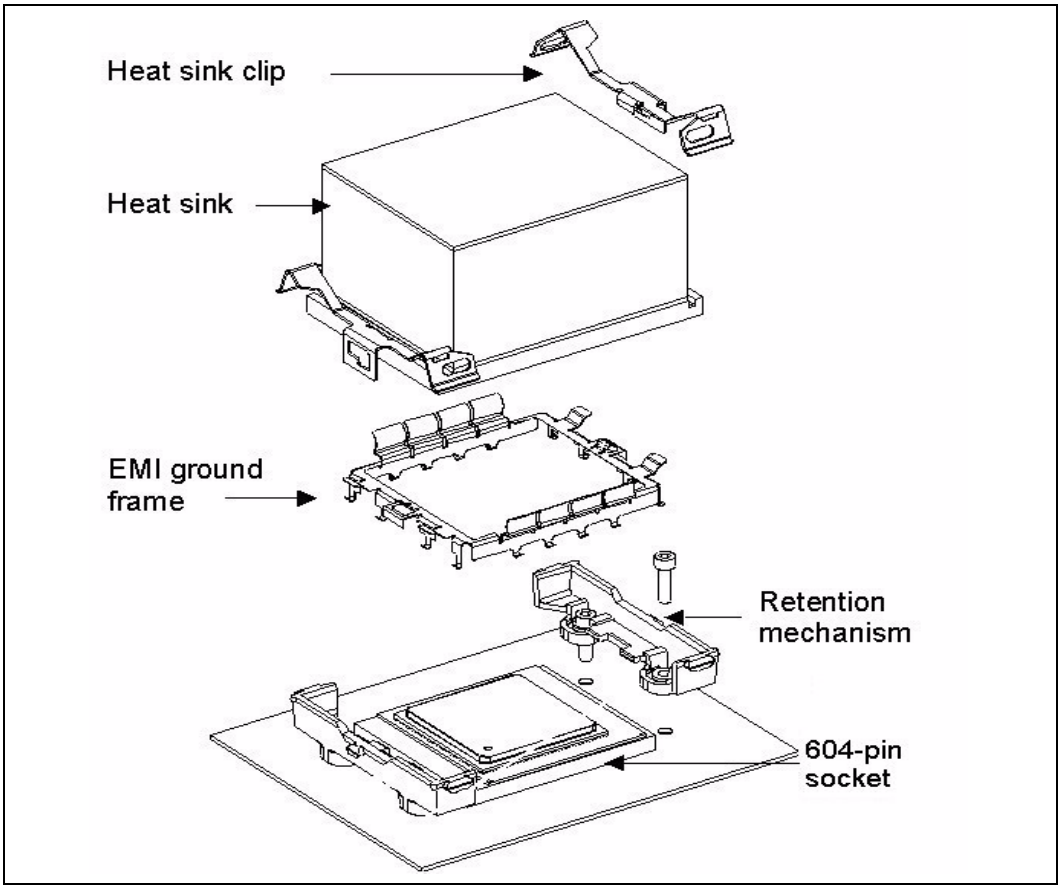
6.0 Thermal Specifications

This chapter provides the thermal specifications necessary for designing a thermal solution for the Low Voltage Intel® Xeon™ processor. Thermal solutions should include heatsinks that apply pressure to the integrated low voltage heat spreader (IHS). The IHS provides a common interface intended to be compatible with many heatsink designs. Thermal specifications are based on the temperature of the IHS top, referred to as the case temperature, or T_{CASE}. Thermal solutions should be designed to maintain the processor within T_{CASE} specifications. For information on performing T_{CASE} measurements, refer to the *Intel® Xeon™ Processor Thermal Design Guidelines*.
See Figure 34 for an exploded view of the processor package and thermal solution assembly.

Figure 34. Processor with Thermal and Mechanical Components - Exploded View



Note: This is a graphical representation. For specifications, see each component's respective documentation listed in Section 1.3.

6.1 Thermal Specifications

To allow for the optimal operation and long-term reliability of Intel processor-based systems, the system/processor thermal solution should be designed such that the processor remains between the minimum and maximum case temperature (TC) specifications when operating at or below the

Thermal Design Power (TDP) value listed per frequency in Table 37. Thermal solutions not designed to provide this level of thermal capability may affect the long-term reliability of the processor and system. For more details on thermal solution design, please refer to the appropriate processor thermal design guidelines.

The case temperature is defined at the geometric top center of the processor IHS. Analysis indicates that real applications are unlikely to cause the processor to consume maximum power dissipation for sustained periods of time. Intel recommends that complete thermal solution designs target the Thermal Design Power (TDP) indicated in Table 37 instead of the maximum processor power consumption. The Thermal Monitor feature is intended to help protect the processor in the unlikely event that an application exceeds the TDP recommendation for a sustained period of time. For more details on the usage of this feature, refer to Section 7.3, "Thermal Monitor" on page 96. In all cases, the Thermal Monitor feature must be enabled for the processor to remain within specification.

Table 37. Processor Thermal Design Power

Core Frequency	Thermal Design Power† (W)	Minimum T_{CASE} (°C)	Maximum T_{CASE} (°C)
1.60 GHz	30	5	81
2.0 GHz	35	5	83
2.4 GHz	40	5	81

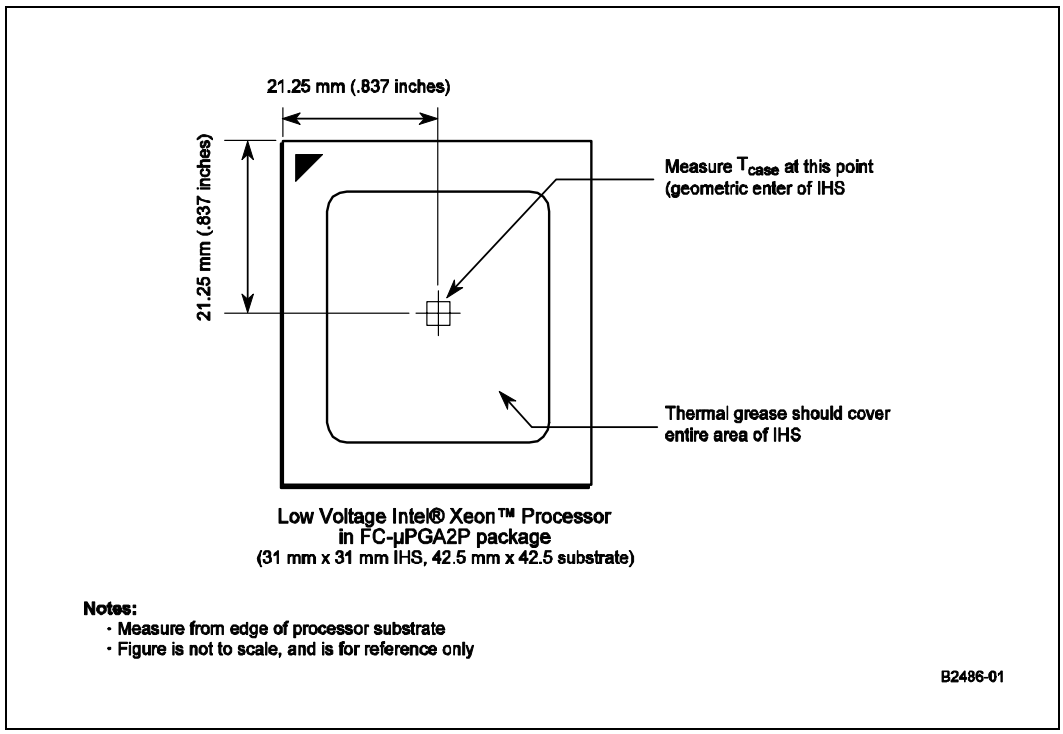
† Intel recommends that thermal solutions be designed utilizing the Thermal Design Power values. Refer to the *Low Voltage Intel® Xeon™ Processor Thermal Design Guidelines* for more information.

6.2 Measurements for Thermal Specifications

6.2.1 Processor Case Temperature Measurement

The maximum and minimum case temperature (T_{CASE}) for the Intel® Xeon™ processor is specified in Table 37. This temperature specification is meant to help ensure proper operation of the processor. Figure 35 on page 91 illustrates where Intel recommends TCASE thermal measurements should be made.

Figure 35. Thermal Measurement Point for Processor T_{CASE}



NOTES:
1. Measure from edge of processor substrate.
2. Figure is not to scale and is for reference only.

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7.0 Features

7.1 Power-On Configuration Options

The Low Voltage Intel® Xeon™ processor has several configuration options that are determined by the state of specific processor pins at the active-to-inactive transition of the processor RESET# signal. These configuration options cannot be changed except by another reset. Both power on and software induced resets reconfigure the processor(s).

Table 38. Power-On Configuration Option Pins

Configuration Option	Pin[1]	Notes
Output tri state	SMI#	
Execute BIST (Built-In Self Test)	INIT#	
In Order Queue de-pipelining (set IOQ depth to 1)	A7#	
Disable MCERR# observation	A9#	
Disable BINIT# observation	A10#	
APIC cluster ID (0-3)	A[12:11]#	2
Disable bus parking	A15#	
Disable Hyper-Threading Technology	A31#	
Symmetric agent arbitration ID	BR[3:0]#	3

NOTES:
1. Asserting this signal during active-to-inactive edge of RESET# may select the corresponding option.
2. The Low Voltage Intel Xeon processor does not support this feature, therefore platforms utilizing this processor should not use these configuration pins.
3. The Low Voltage Intel Xeon processor utilizes only BR0# and BR1# signals. Two-way platforms must not utilize BR2# and BR3# signals.

7.2 Clock Control and Low Power States

The processor allows the use of AutoHALT, Stop-Grant and Sleep states to reduce power consumption by stopping the clock to internal sections of the processor, depending on each particular state. See Figure 36 for a visual representation of the processor low power states.

Due to the inability of processors to recognize bus transactions during the Sleep state, multiprocessor systems are not allowed to simultaneously have one processor in Sleep state and the other processor in the Normal or Stop-Grant state.

7.2.1 Normal State—State 1

This is the normal operating state for the processor.

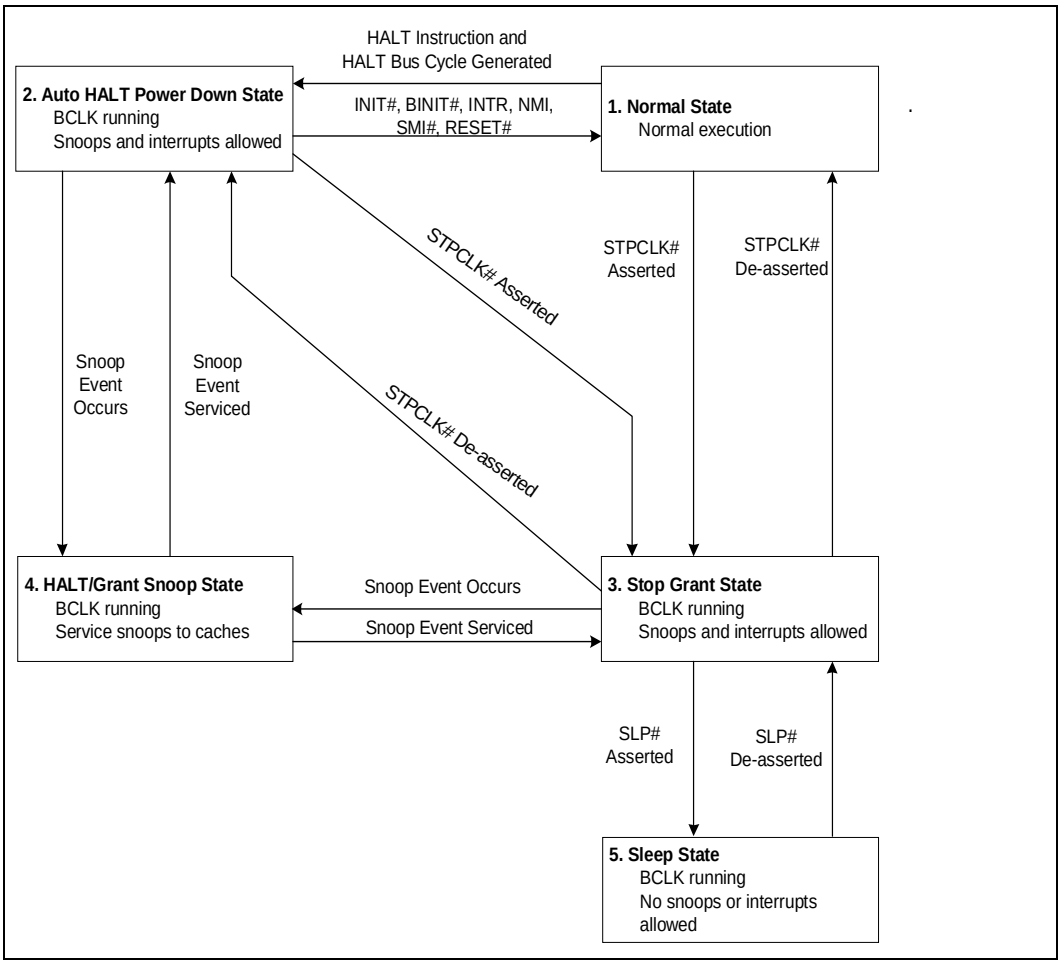
7.2.2 AutoHALT Powerdown State—State 2

AutoHALT is a low power state entered when the processor executes the HALT instruction. The processor may transition to the Normal state upon the occurrence of SMI#, BINIT#, INIT#, LINT[1:0] (NMI, INTR), or an interrupt delivered over the system bus. RESET# may cause the processor to immediately initialize itself.

The return from a System Management Interrupt (SMI) handler may be to either Normal Mode or the AutoHALT Power Down state. See the *Intel Architecture Software Developer's Manual, Volume III: System Programmer's Guide* for more information.

The system may generate a STPCLK# while the processor is in the AutoHALT Power Down state. When the system deasserts the STPCLK# interrupt, the processor may return execution to the HALT state.

Figure 36. Stop Clock State Machine



7.2.3 Stop-Grant State—State 3

When the STPCLK# pin is asserted, the Stop-Grant state of the processor is entered 20 bus clocks after the response phase of the processor-issued Stop Grant Acknowledge special bus cycle. Once the STPCLK# pin has been asserted, it may only be deasserted once the processor is in the Stop Grant state. Both logical processors of the Low Voltage Intel Xeon processor must be in the Stop Grant state before the deassertion of STPCLK#.

Since the AGTL+ signal pins receive power from the system bus, these pins should not be driven (allowing the level to return to V_{CC}) for minimum power drawn by the termination resistors in this state. In addition, all other input pins on the system bus should be driven to the inactive state.

BINIT# may be recognized while the processor is in Stop-Grant state. When STPCLK# is still asserted at the completion of the BINIT# bus initialization, the processor may remain in Stop-Grant mode. When STPCLK# is not asserted at the completion of the BINIT# bus initialization, the processor may return to Normal state.

RESET# may cause the processor to immediately initialize itself, but the processor may stay in Stop-Grant state. A transition back to the Normal state may occur with the deassertion of the STPCLK# signal. When re-entering the Stop-Grant state from the sleep state, STPCLK# should only be deasserted one or more bus clocks after the deassertion of SLP#.

A transition to the HALT/Grant Snoop state may occur when the processor detects a snoop on the system bus (see Section 7.2.4). A transition to the Sleep state (see Section 7.2.5) may occur with the assertion of the SLP# signal.

While in the Stop-Grant state, SMI#, INIT#, BINIT# and LINT[1:0] may be latched by the processor, and only serviced when the processor returns to the Normal state. Only one occurrence of each event may be recognized upon return to the Normal state.

7.2.4 HALT/Grant Snoop State—State 4

The processor may respond to snoop transactions on the system bus while in Stop-Grant state or in AutoHALT Power Down state. During a snoop transaction, the processor enters the HALT/Grant Snoop state. The processor may stay in this state until the snoop on the system bus has been serviced (whether by the processor or another agent on the system bus). After the snoop is serviced, the processor may return to the Stop-Grant state or AutoHALT Power Down state, as appropriate.

7.2.5 Sleep State—State 5

The Sleep state is a very low power state in which each processor maintains its context, maintains the phase-locked loop (PLL), and has stopped most of internal clocks. The Sleep state may only be entered from Stop-Grant state. Once in the Stop-Grant state, the SLP# pin may be asserted, causing the processor to enter the Sleep state. The SLP# pin is not recognized in the Normal or AutoHALT states.

Snoop events that occur while in Sleep state or during a transition into or out of Sleep state may cause unpredictable behavior.

In the Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals (with the exception of SLP# or RESET#) are allowed on the system bus while the processor is in Sleep state. Any transition on an input signal before the processor has returned to Stop-Grant state may result in unpredictable behavior.

When RESET# is driven active while the processor is in the Sleep state, and held active as specified in the RESET# pin specification, the processor may reset itself, ignoring the transition through Stop-Grant state. When RESET# is driven active while the processor is in the Sleep state, the SLP# and STPCLK# signals should be deasserted immediately after RESET# is asserted to ensure the processor correctly executes the reset sequence.

Once in the Sleep state, the SLP# pin may be deasserted when another asynchronous system bus event occurs. The SLP# pin should only be asserted when the processor (and all logical processors within the physical processor) is in the Stop-Grant state. SLP# assertions while the processors are not in the Stop-Grant state is out of specification and may result in illegal operation.

7.2.6 Bus Response During Low Power States

While in AutoHALT Power Down and Stop-Grant states, the processor may process a system bus snoop.

When the processor is in Sleep state, the processor may not process interrupts or snoop transactions.

7.3 Thermal Monitor

The Thermal Monitor feature helps control the processor temperature by activating the Thermal Control Circuit (TCC) when the processor silicon reaches its maximum operating temperature. The TCC reduces processor power consumption by modulating (starting and stopping) the internal processor core clocks. The Thermal Monitor feature must be enabled for the processor to be operating within specifications. The temperature at which Thermal Monitor activates the thermal control circuit is not user configurable and is not software visible. Bus traffic is snooped in the normal manner, and interrupt requests are latched (and serviced during the time that the clocks are on) while the TCC is active.

When the Thermal Monitor feature is enabled, and a high temperature situation exists (i.e., TCC is active), the clocks will be modulated by alternately turning the clocks off and on at a duty cycle specific to the processor (typically 30 to 50 percent). Frequently, clocks will not be off for more than 3.0 microseconds when the TCC is active. Cycle times are processor speed dependent and will decrease as processor core frequencies increase. A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near its maximum operating temperature. Once the temperature has dropped below the maximum operating temperature, and the hysteresis timer has expired, the TCC goes inactive and clock modulation ceases.

With a properly designed and characterized thermal solution, it is anticipated that the TCC would only be activated for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be so minor that it would be immeasurable. An under-designed thermal solution that is not able to prevent excessive activation of the TCC in the anticipated ambient environment may cause a noticeable performance loss, and in some cases may result in a TC that exceeds the specified maximum temperature and may affect the long-term reliability of the processor. In addition, a thermal solution that is significantly under-designed may not be capable of cooling the processor even when the TCC is active continuously. Refer to the Intel® Xeon™ Processor Thermal Design Guidelines for information on designing a thermal solution.

The duty cycle for the TCC, when activated by the Thermal Monitor, is factory configured and cannot be modified. The Thermal Monitor does not require any additional hardware, software drivers, or interrupt handling routines.

7.3.1 Thermal Diode

The processor incorporates an on-die thermal diode. A thermal sensor located on the processor may be used to monitor the die temperature of the processor for thermal management/long term die temperature change purposes. This thermal diode is separate from the Thermal Monitor's thermal sensor and cannot be used to predict the behavior of the Thermal Monitor.

7.4 Thermal Diode

The Low Voltage Intel Xeon processor incorporates an on-die thermal diode. A thermal sensor located on the baseboard may monitor the die temperature of the processor for thermal management/long term die temperature change purposes. Table 39 and Table 40 provide the diode parameter and interface specifications. This thermal diode is separate from the Thermal Monitor's thermal sensor and cannot be used to predict the behavior of the Thermal Monitor.

Table 39. Thermal Diode Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I_{FW}	Forward Bias Current	5		300	µA	1
n	Diode Ideality Factor	1.0011	1.0021	1.0030		2, 3, 4
R_T	Series Resistance		3.64		W	2, 3, 5

NOTES:
1. Intel does not support or recommend operation of the thermal diode under reverse bias.
2. Characterized at 75°C.
3. Not 100% tested. Specified by design characterization.
4. The ideality factor, n, represents the deviation from ideal diode behavior as exemplified by the diode equation:
   $I_{FW}=I_S *(e^{(qV_D/nkT)} -1)$
   Where I_S = saturation current, q = electronic charge, V_D = voltage across the diode, k = Boltzmann Constant, and T = absolute temperature (Kelvin).
5. The series resistance, R_T, is provided to allow for a more accurate measurement of the diode junction temperature. R_T as defined includes the pins of the processor but does not include any socket resistance or board trace resistance between the socket and the external remote diode thermal sensor. R_T may be used by remote diode thermal sensors with automatic series resistance cancellation to calibrate out this error term. Another application is that a temperature offset may be manually calculated and programmed into an offset register in the remote diode thermal sensors as exemplified by the equation:
   $T_{error} = [R_T*(N-1)*I_{FWmin}]/[(nk/q)*\ln N]$
   Where T_{error} = sensor temperature error, N = sensor current ration, k = Boltzmann Constant, q = electronic charge.

Table 40. Thermal Diode Interface

Pin Name	Pin Number	Pin Description
THERMDA	Y27	diode anode
THERMDC	Y28	diode cathode

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8.0 Debug Tools Specifications

The Debug Port design information has been moved. This includes all information necessary to develop a Debug Port on this platform, including electrical specifications, mechanical requirements, and all In-Target Probe (ITP) signal layout guidelines. Please reference the *ITP700 Debug Port Design Guide* for the design of your platform.

8.1 Logic Analyzer Interface (LAI)

Intel® is working with two logic analyzer vendors to provide logic analyzer interfaces (LAIs) for use in debugging systems. Tektronix* and Agilent* should be contacted to get specific information about their logic analyzer interfaces. The following information is general in nature. Specific information must be obtained from the logic analyzer vendor.

Due to the complexity of systems, the LAI is critical in providing the ability to probe and capture system bus signals. There are two sets of considerations to keep in mind when designing a system that may make use of an LAI: mechanical and electrical.

8.1.1 Mechanical Considerations

The LAI is installed between the processor socket and the processor. The LAI pins plug into the socket, while the processor pins plug into a socket on the LAI. Cabling that is part of the LAI egresses the system to allow an electrical connection between the processor and a logic analyzer. The maximum volume occupied by the LAI, known as the keepout volume, as well as the cable egress restrictions, should be obtained from the logic analyzer vendor. System designers must make sure that the keepout volume remains unobstructed inside the system. Note that it is possible that the keepout volume reserved for the LAI may differ from the space normally occupied by the processor heatsink. When this is the case, the logic analyzer vendor may provide a cooling solution as part of the LAI.

8.1.2 Electrical Considerations

The LAI may also affect the electrical performance of the system bus; therefore, it is critical to obtain electrical load models from each of the logic analyzers to be able to run system level simulations to prove that their tool may work in the system. Contact the logic analyzer vendor for electrical specifications and load models for the LAI solution they provide.

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9.0 Appendix A

9.1 Processor Core Frequency Determination

To allow system debug and multiprocessor configuration flexibility, the core frequency of the processor may be configured using an MSR.

Clock multiplying within the processor is provided by the internal Phase Lock Loop (PLL), which requires a constant frequency BCLK inputs. For Spread Spectrum Clocking, please refer to the *CK00 Clock Synthesizer/Driver Design Guidelines* and the *CK408 Clock Synthesizer/Driver Design Guidelines*. The system bus frequency ratio cannot be changed dynamically during normal processor operation, nor can it be changed during any low power modes. The system bus frequency ratio can be changed when RESET# is active, assuming that all Reset specifications are met. However, the reprogrammed values will not take effect until after the processor has undergone a warm RESET.

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